Investigating the Polyimide-Copper Interface to Improve Modeling and Design in Advanced Semiconductor Packages.

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Project Motivation

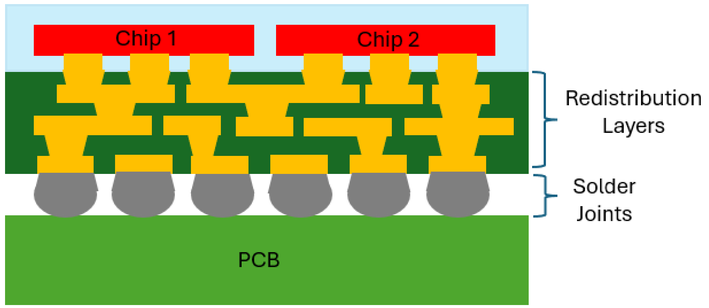

Figure 1: 2D Cross Section of a Semiconductor Package

Advanced semiconductor packaging is a collection of methods to connect and encapsulate computer chips to improve computational performance, manage heat, reduce power consumption, and fit into smaller spaces. A critical aspect of this is the use of copper redistribution layers (RDL), thin metal wires embedded in the package that connect chip(s) together with the input and output connections.

Research Objectives

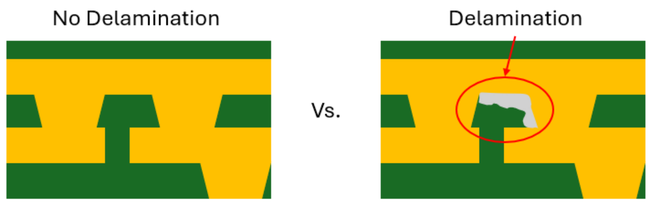

Figure 2: 2D Cross Sections Showing Delamination vs No Delamination

Delamination at the polyimide-copper interface can compromise mechanical reliability and disrupt electrical pathways, causing device failure. To better understand and prevent this issue, the objectives for the investigation are:

- Measure interfacial adhesion and fracture energy using double cantilever beam (DCB) and peel testing.
- Use experimental data to develop and calibrate a simulation workflow in ANSYS.

Experimental Methodology

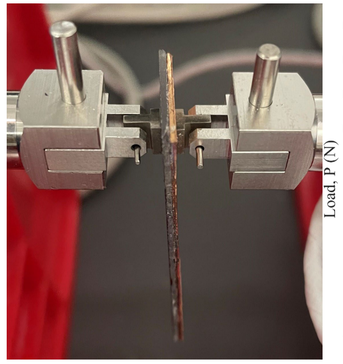

Figure 3: Dual Cantilever Beam Testing Apparatus

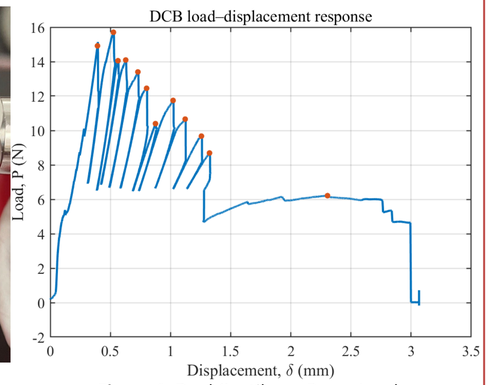

Figure 4: Dual Cantilever Beam Load-Displacement Plot

Double cantilever beam (DCB) testing is a method to measure adhesion strength and interfacial fracture energy. Two bonded components (copper and polyimide) are mechanically separated while the load required to maintain constant displacement is measured, causing a pre-existing crack to propagate through the sample along the interface.

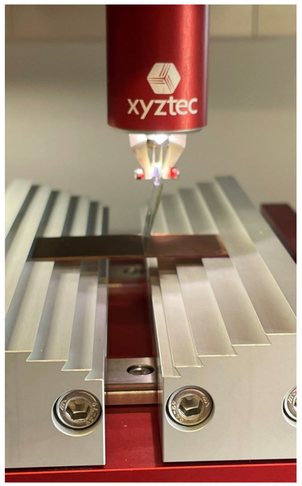

Figure 5: Peel Testing Apparatus

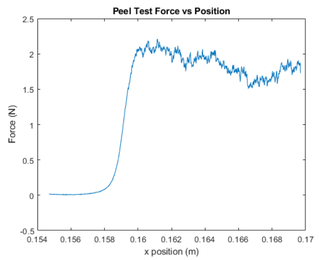

Figure 6: Peel Testing Force Displacement results

Peel testing is another method to measure adhesion strength at the interface. While it does not capture the interfacial fracture toughness like a DCB test, it is able to examine things like how the peeled material's elastic properties affect how the separation along the interface proceeds.

Simulation Methodology

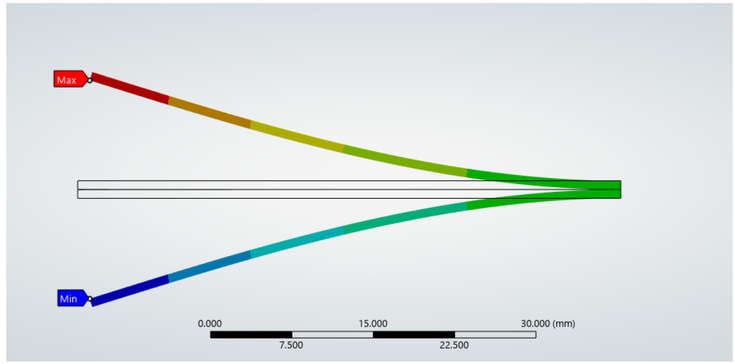

Figure 7: Ansys Simulation of DCB Test Using Cohesive Zone Modeling

Data from the DCB testing was loaded into ANSYS and used to recreate the DCB test in a simulation; the resulting data can be compared to the physical experimental data to calibrate the ANSYS workflow.

Future Work

To expand the scope of this investigation with additional time, future work will focus on expanding the experimental scope and simulation validation:

- Investigate electroplated copper that is more representative of materials in a real semiconductor package.
- Expand peel testing to include smaller copper features deposited onto a pre-existing polyimide surface.
- Use the data from these experiments to continue developing and validating simulation workflows.

Applications

The information collected on the polyimide-copper interface can help inform models and digital representations of the interface. By using experimental data to verify and calibrate simulations, this investigation starts the process of creating a digital twin. When integrated into design tools, a digital twin can assist in designing reliable RDL in advanced semiconductor packages to improve reliability, cost, and performance.

FURI

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