Conductive Filament Modeling and Reliability Prediction in Pt/SiO_x/TiN Resistive Random Access Memory

Andrew Rubio, Electrical Engineering
Mentor(s): Dr. Ying-Chen Daphne Chen, Assistant Professor
School of Electrical, Computer and Energy Engineering (ECEE), Arizona State University

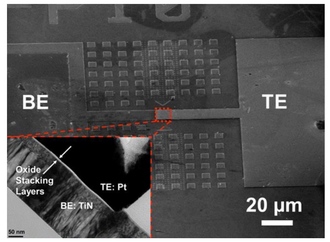
Motivation

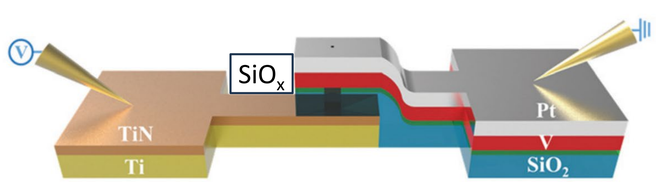
Modern computing faces an issue with the von Neumann architecture, where the power consumption between data transfer from memory to CPU causes a limitation on computing efficiency. Emerging memory, namely Resistive Random Access Memory (ReRAM), technology has been proposed as the device to overcome this bottleneck. Applications such as high-density storage memory and computational functions will be used towards AI and post CMOS era.

In this study: The resistive switching behaviors on Pt/SiO_x (11 nm)/TiN RRAM devices were fabricated by RF sputtering with retention characterized with device area dependency of 0.4 and 0.6 μm.

Background

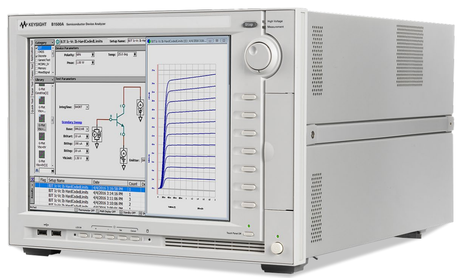
- Oxide-based ReRAM operates by forming and rupturing a conductive filament under forward or reverse bias, switching between low and high resistance states.
- Reliability of these devices are dependent on two characteristics: **endurance** and **retention**, further explained as the amount of DC cycles they can operate and how long they can retain their state, respectively.



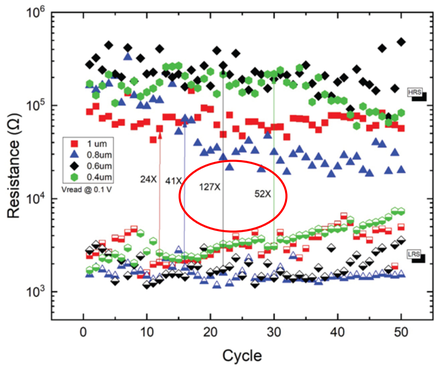


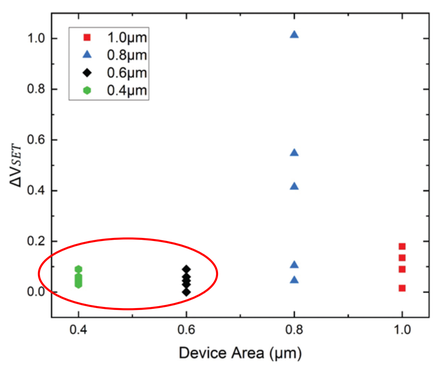
Methodology

- DC cycling between SET and RESET processes were conducted to stabilize devices for retention testing.
- Retention data was collected at 0.1V V_{READ} over the course of 3 hours for each resistance state.
- A FormFactor S200 probe station and Keysight B1500A Semiconductor Device Parameter Analyzer were used for device characterization.



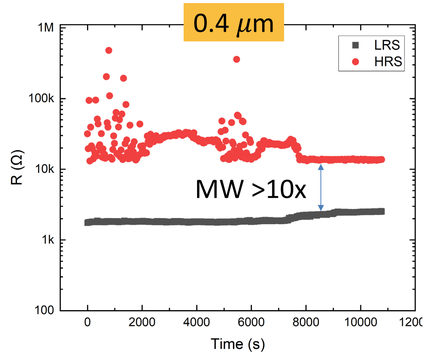
Device Endurance Performance

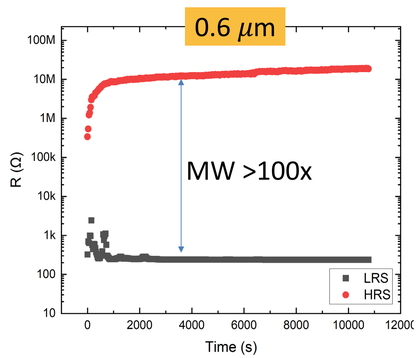




- 0.4 μm and 0.6 μm devices were previously found to exhibit great DC endurance, making them interesting candidates for device retention

Results and Future Work





- Results show great DC Retention and stability in the LRS of both 0.4 and 0.6 μm devices.
- Small instabilities were observed in HRS, though kept within same order of magnitude.
- To further understand switching mechanisms and reliability in Pt/SiO_x/TiN, linear fitting of the I-V curves will be conducted. Current transport mechanisms will further explain the role of oxygen vacancies within the device.

Conclusion

- **SiO_x-based RRAM with device area dependency has further been studied for high density storage, neuromorphic computing, and CMOS compatible BEOL integration.**
- **Pt/SiO_x/TiN devices of area 0.6 μm continue to show a large memory window (>100), great DC retention for 3 hours, and less resistance state variation.**
- **HRS variation mechanisms/behavior in retention will further be studied.**

FURI

SDRL Semiconductors and Device Research Lab

ASU Ira A. Fulton Schools of Engineering
Arizona State University