A Switched-Resistor Array for Pulsed-Power Load Emulation

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Research Question

How do we model a switched-resistor array for the design of a pulsed load emulator?

Background

My previous work [1] showed that a switched-resistor array (Fig. 1) is a promising solution for the design of a point-of-load pulse emulator with the specifications enumerated in Table 1. The performance of the proposed design is limited by resistor ESL, GaNFET output capacitance, and inductance from the physical layout of the board.

Table 1: Pulsed Load Specifications

f	D	V	P
10kHz-200kHz	1%-30%	18V-36V	4kW

To design such a load, we need accurate analytical and simulation models. To that end, this work develops a small-scale version of the proposed design to verify design models.

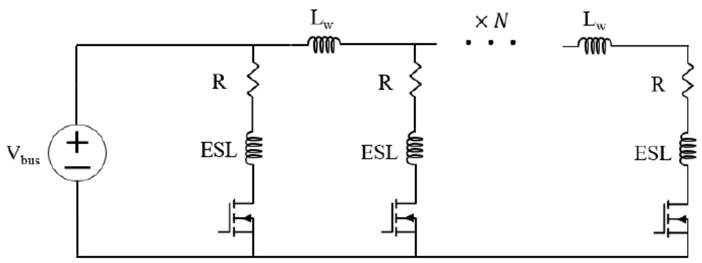

Figure 1: Switched-Resistor Array with Parasitic Inductances Shown

Proposed Design

By virtue of the GaNFET, the turn-on and turn-off of the pulse are asymmetric. Namely, the turn-on is modeled as a series RL circuit with the GanFET modeled by its on-resistance; the turn-off is modeled as a series RLC circuit with the GaNFET modeled by its output capacitance. This work proposes underdamped (Fig. 3) and overdamped (Fig. 4) designs.

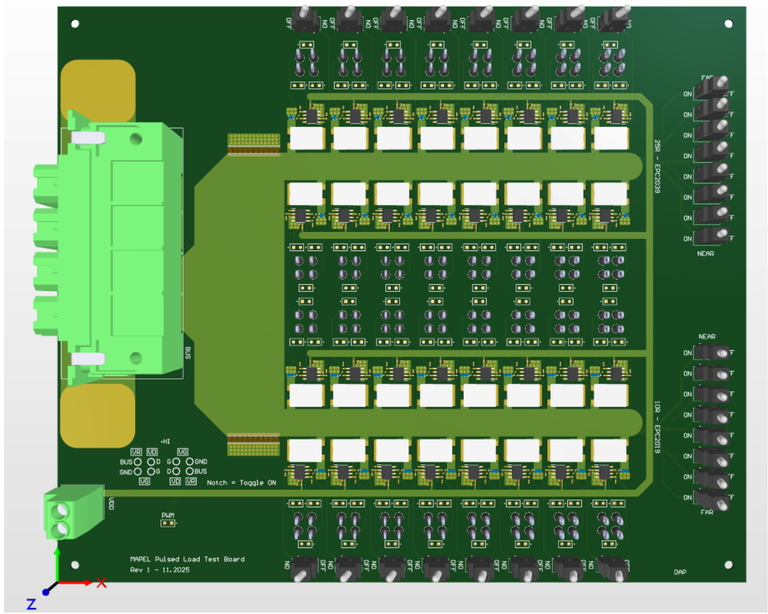

Figure 2: 3-D Rendering of Pulsed Load Test Board (Altium)

The above figure shows the printed circuit board (PCB) that will be used to verify design models.

LTspice Simulation Results

The figures below show the simulation results using a manufacturer-provided GaNFET spice model for a switched-resistor array with five resistors and the following parameters: ESL=14.5nH, L_w=0.35nH, V=18V, f=200kHz, D=1%. The underdamped design employs 10Ω resistors and EPC-2019 GaN switches; the overdamped design employs 25Ω resistors and EPC-2039 GaN switches.

Figure 3: Load Current (Underdamped Design)

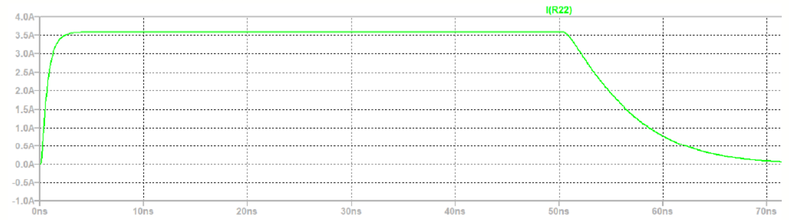

Figure 4: Load Current (Overdamped Design)

Future Work

Assemble the test board and collect experimental data to verify design models. Then, design, build, and test the full-power version.

References

[1] D. A. Puerta and M. K. Ranjram, "Point-of-Load Pulse Emulator for High-Performance Testing," poster presented at *Fulton Forge Research Expo*, Arizona State University, Apr. 2025. [Online]. Available: https://forge.engineering.asu.edu/furiproject/point-of-load-pulse-emulator-for-high-performance-power-converter-testing/

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