Identifying Current Transport Mechanisms in Resistive Random Access Memory for Reliability Investigation

Jordan Dunn, Electrical Engineering
Mentor: Ying-Chen Daphne Chen
School of Electrical, Computer and Energy Engineering (ECEE)

Research Question

How can the current transport mechanisms of a Metal-Insulator-Metal bilayer RRAM device be determined from raw data and an I-V curve then compared to a single layer Metal-Insulator-Metal RRAM device?

Methods

Resistive Random Access Memory Device Structure (Selectorless RRAM & 2D RRAM)

- Pt/HfOx/SiOx/TiN and vdw CIPS devices

Data Gathering

- This research investigated 0.4 um and 0.6 um devices and the FormFactor Manual MPS150 probe station was used to probe the chip and collect data. Three devices from each feature sizes were chosen and the RESET voltage was found for all of the selected devices. These devices were then cycled 30 times each and their I-V curves were examined on the Keysight B1500A Analyzer

Analysis

- The slope and R squared value were extracted from the linear fit plots
- These values were then examined, and each cycle was assigned its dominating transport mechanism based off Table 1

Overview

Charge transport	I	G_N	Linear fitting plots	Slope
Poole – Frenkel	$gVe^{\beta\sqrt{V}}$	$1+\beta\sqrt{V}/2$	$Ln(I/V)$ vs $V^{1/2}$	-
Fowler-Nordheim	$AV^2e^{-B/V}$	$2+B/V$	$Ln(I/V^2)$ vs $(1/V)$	-
Schottky	$I_oe^{P\sqrt{V}}$	$P\sqrt{V}/2$	$Ln(I)$ vs $V^{1/2}$	-
Hopping	KVe^{LV}	$1 + LV$	$Ln(I/V)$ vs V	-
Power law	MV^p	P	$Ln(I)$ vs $Ln(V)$	-
Ohmic	-	-	$Ln(I)$ vs $Ln(V)$	1
Space Charge Limited current (SCLC)	V^2	-	$Ln(I)$ vs $Ln(V)$	2

Table 1: The seven charge transport mechanisms and their corresponding linear fit equations

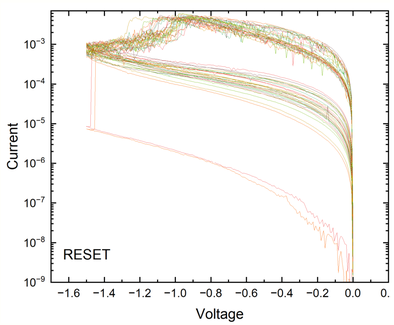


Figure 2: RESET process for 0.6um device

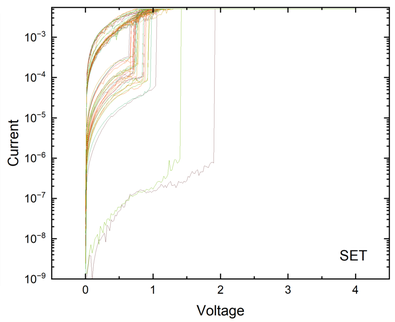
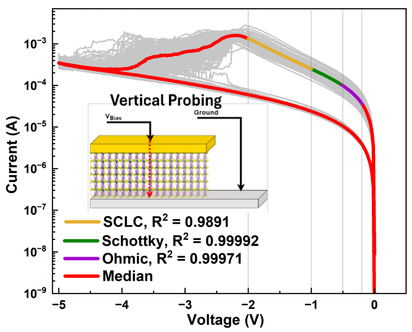


Figure 3: SET process for 0.6um device



RESET region of the device (190 DC cycles) with colored three regions for numerical current fitting

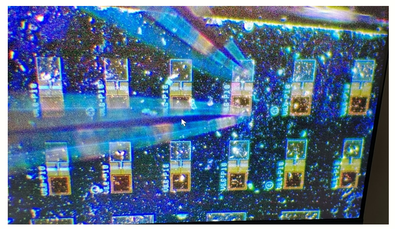


Figure 1: 0.4 and 0.6 µm devices under a microscope

Results

After testing the devices and analyzing their I-V curves, it could be seen that they exhibited a large and stable memory window. The low resistance state for both the SET and RESET portion of the curve appeared to be non-linear. This suggests space charge limited current transport mechanism. Comparing to a Pt/SiOx/TiN device, this Pt/HfOx/SiOx/TiN device appears to be more stable.

Conclusion

This project taught important methods on how to operate a probe station and analyze data. This nonlinear behavior is beneficial for selectorless RRAM in large density array applications toward low power AI.

References

Chen, Ying-Chen, et al. “Internal filament modulation in low-dielectric gap design for built-in selector-less resistive switching memory application.” *Journal of Physics D: Applied Physics*, vol. 51, no. 5, 16 Jan. 2018, p. 055108, https://doi.org/10.1088/1361-6463/aaa1b9.

Future Work and Acknowledgements

The future work of this project includes further electrical characterization testing of 0.8 um and 1.0 um devices by using probe stations.

FURI

SDRL Semiconductors and Device Research Lab

Ira A. Fulton Schools of Engineering
Arizona State University