

# Programmable 2D Perovskite Memristors for Computing Hardware

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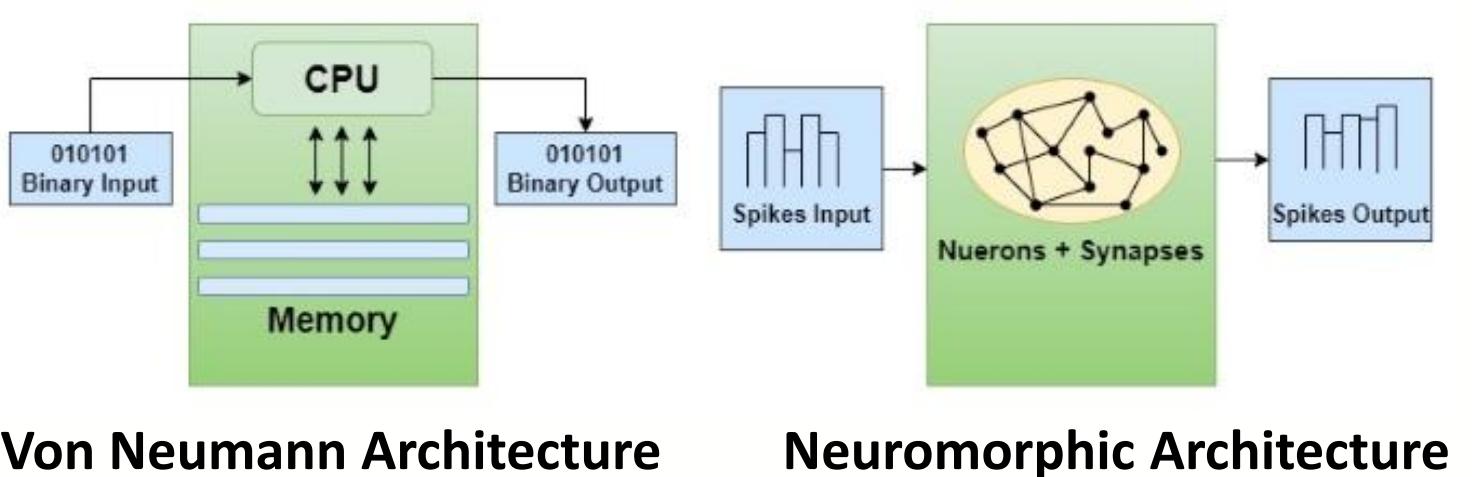
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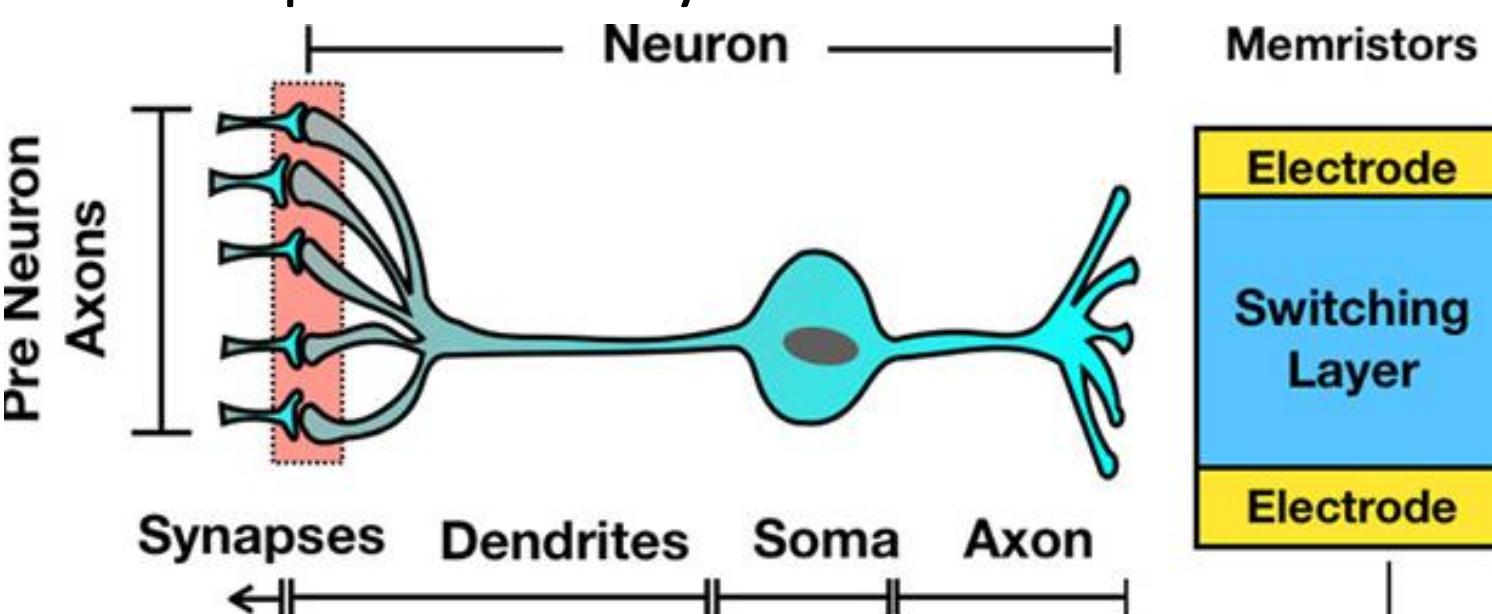
## Introduction & Background

- A memristor is a memory device that stores data by changing its conductance. It functions as an artificial synapse for neuromorphic computing systems, which offer a low-power alternative to conventional von Neumann computing architectures.



Von Neumann Architecture      Neuromorphic Architecture

- Halide perovskites are promising memristive materials due to their mixed ionic-electronic conductivity and homogenous ion migration. However, traditional 3D perovskites are limited by poor moisture stability and nonlinear resistive programming. While standard 2D perovskites solve the moisture resistance problem, they still suffer from asymmetrical and nonlinear conductance changes that limit their accuracy in computing applications.
- The device is programmed using a sequence of electrical pulses, with positive pulses causing a gradual conductance increase and negative pulses causing a gradual decrease. This switching simulates a synaptic weight and is physically caused by the controlled, homogeneous migration of charged ions throughout the entire perovskite crystal.



## Acknowledgements

I would like to thank Dr Nicholas Rolston and Vineeth Penukula for their continued guidance and mentorship

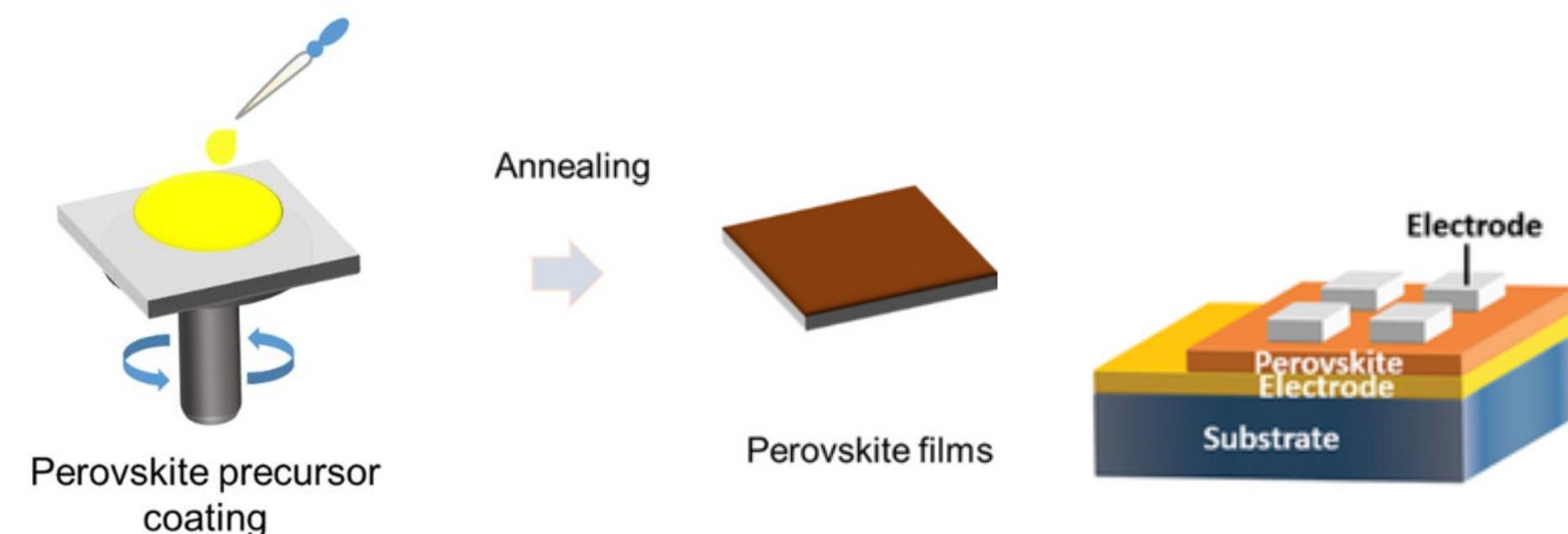
## References

Kim, S.J., Im, I.H., Baek, J.H. et al. Linearly programmable two-dimensional halide perovskite memristor arrays for neuromorphic computing. *Nat. Nanotechnol.* 20, 83–92 (2025). <https://doi.org/10.1038/s41565-024-01790-3>

Alamban, A., Ahmad, M., & Rolston, N. (2024). 2D Ruddlesden–Popper Perovskites with Polymer Additive as Stable and Transparent Optoelectronic Materials for Building-Integrated Applications. *Nanomaterials*, 14(14), 1184. <https://doi.org/10.3390/nano14141184>

## Methodology

- The Dion-Jacobson phase 2D perovskite precursor solution,  $\text{PDAMA}_{n-1}\text{Pb}_n\text{I}_{3n+1}$ , was prepared by stirring  $\text{PbI}_2$ ,  $\text{MAI}$ , and  $\text{PbI}_2$  powders in anhydrous DMF for 1 hour.
- The solution was spin-coated onto an ITO/glass substrate at 4,000 rpm for 30 s, followed by annealing at 100 degrees Celsius for 15 min.
- An ultrathin PMMA layer was spin-coated on the perovskite film. Finally, a gold paste was applied to create the Au top electrodes, completing the device structure.
- Electrical properties like the J-V curve were measured using FLUXiM Paios Module.



## Results

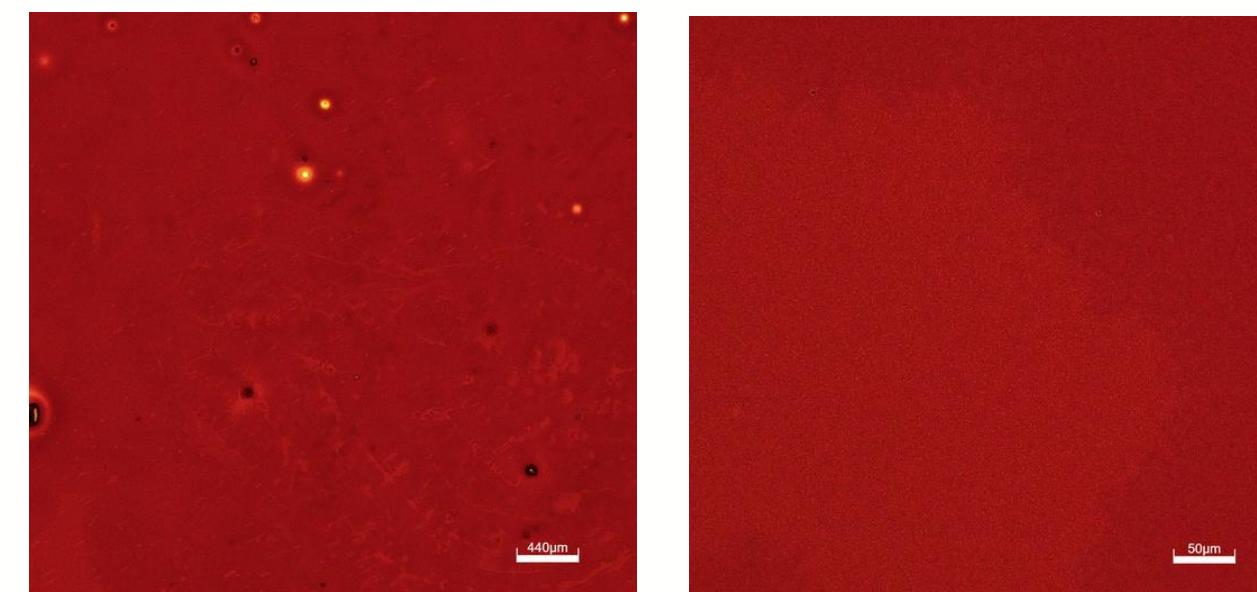


Fig. 1 Microscope images of the  $\text{PDAMA}_1\text{Pb}_2\text{I}_7$  film.

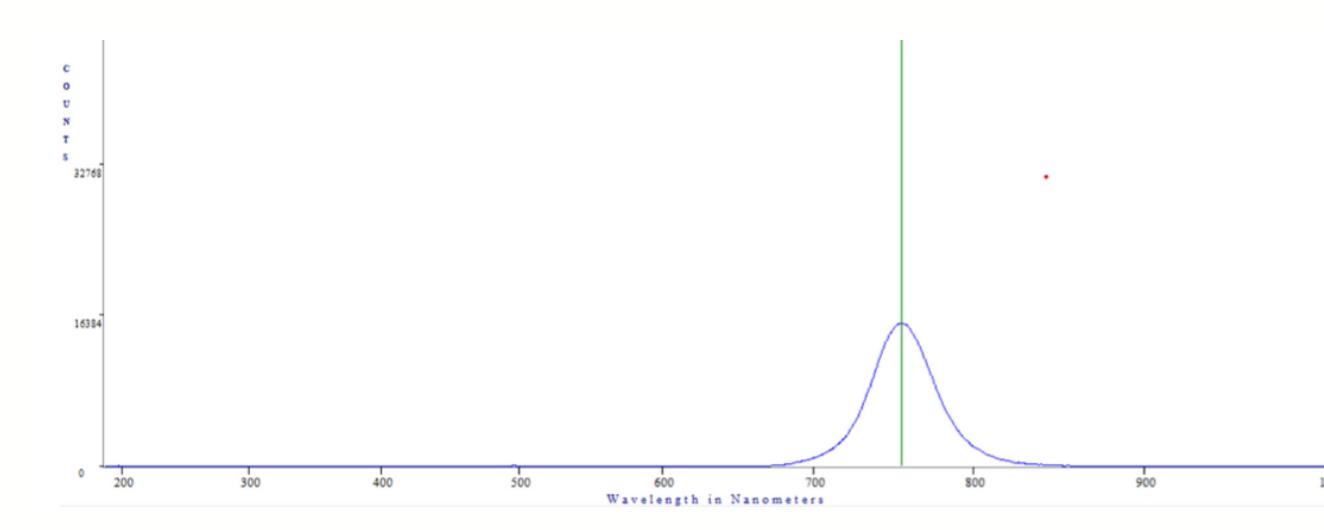


Fig. 2 Photoluminescence spectrum of the  $\text{PDAMA}_1\text{Pb}_2\text{I}_7$  film, showing the emission peak.

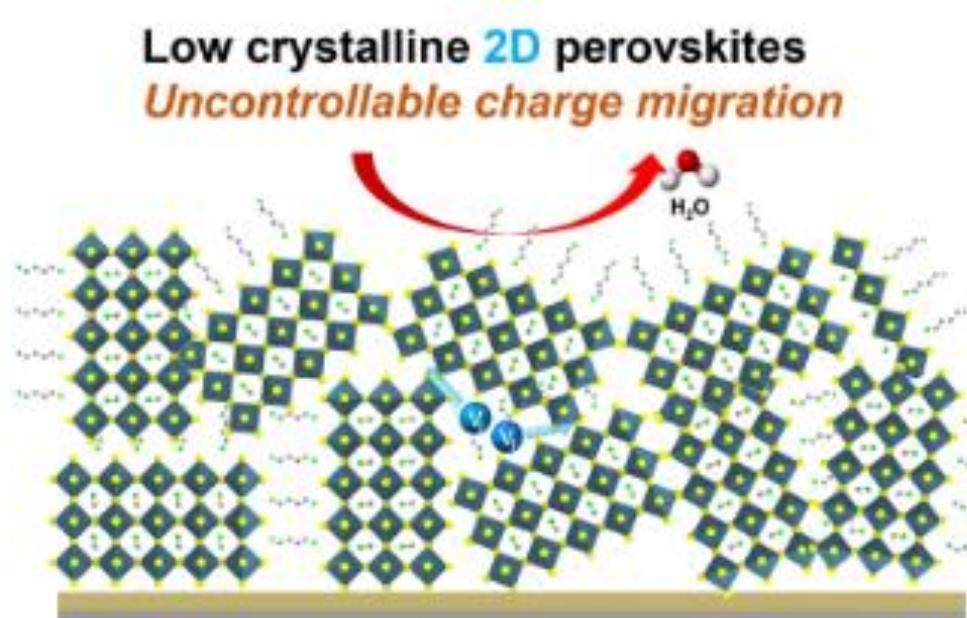


Fig. 3 Randomly oriented film

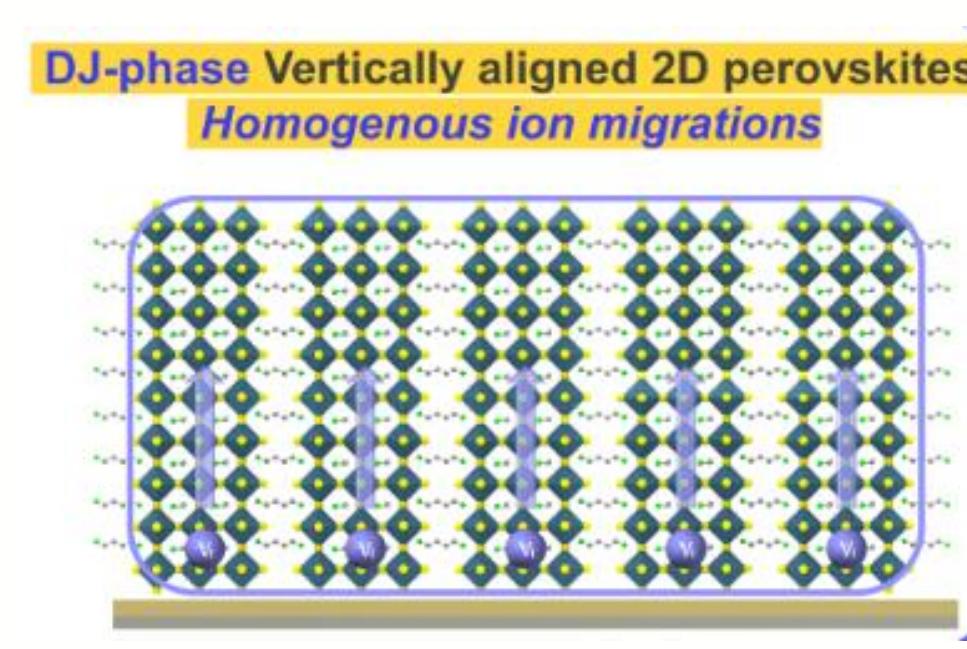


Fig. 4 Vertically aligned DJ-Phase film

## Discussion

- Optical images and a single, sharp PL peak at ~750 nm confirm the successful synthesis of a high-quality, pure-phase  $\text{PDAMA}_1\text{Pb}_2\text{I}_7$  film.
- Without an additive, the perovskite film forms as a low-crystallinity film with a random crystal orientation, as illustrated in Fig. 3.
- 2D perovskites are structured with conductive inorganic layers separated by insulating organic spacer layers. In this random, non-aligned state, these insulating organic layers act as barriers, blocking the vertical flow of current between the top and bottom electrodes.
- This highly resistive, defective film explains the poor performance of memristive switching and proves that vertical alignment (Fig. 4) is essential.

## Outlook

- Incorporate additives to promote vertical crystal alignment, which is essential for stable and linear switching.
- Explore other 2D perovskite compositions and different electrode materials to optimize device performance.
- The ultimate goal is to scale up from single devices to large-scale  $n \times n$  crossbar arrays for practical neuromorphic computing. This will require developing new fabrication techniques because perovskites are incompatible with traditional photolithography.

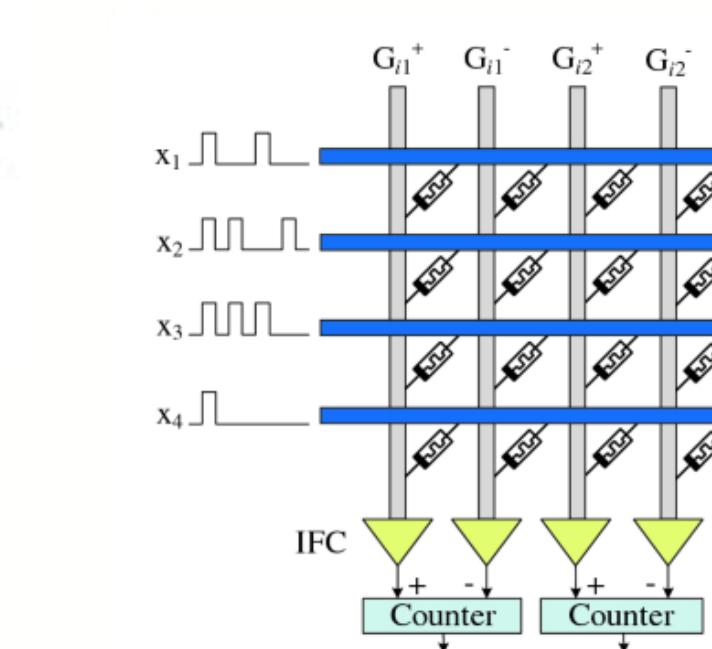


Fig. 5 Spiking neural network array

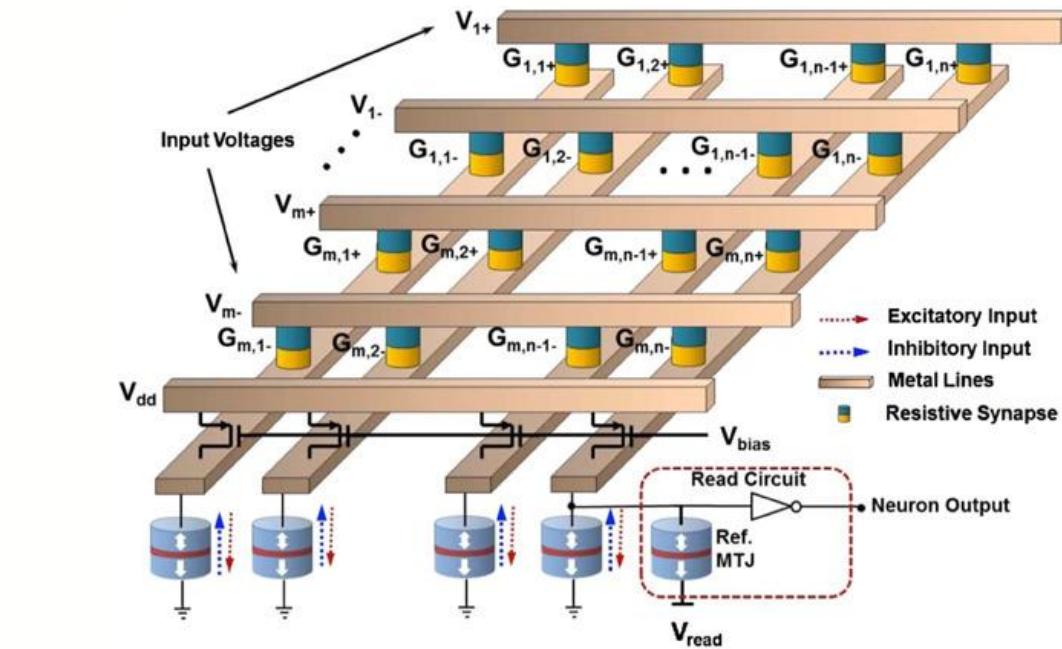


Fig. 6  $n \times n$  memristor crossbar array

These arrays, as shown in the target architecture (Fig. 6), would integrate our memristors as resistive synapses with read circuits. They would then be programmed using brain-inspired spike inputs ( $x_1, x_2, \dots$  in Fig. 5) to perform efficient, in-memory computations.