VeriLLM: A Large Language Model-Driven Toolchain for Enhanced Verilog Workflow Optimization

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Background

Verilog, a hardware description language, is essential for digital circuit design, but current datasets are too simplistic for large language models (LLMs) to handle complex, real-world tasks. **Intuitor** addresses this by using **self-reward training**, inspired by *Learning without External Rewards* [1], where the model learns to minimize KL-divergence across multiple responses to increase self-confidence without external labels.

Methodology

VeriLLM fine-tunes a QWEN3-14B model using **self-reward training** via the **Intuitor** framework shown below.

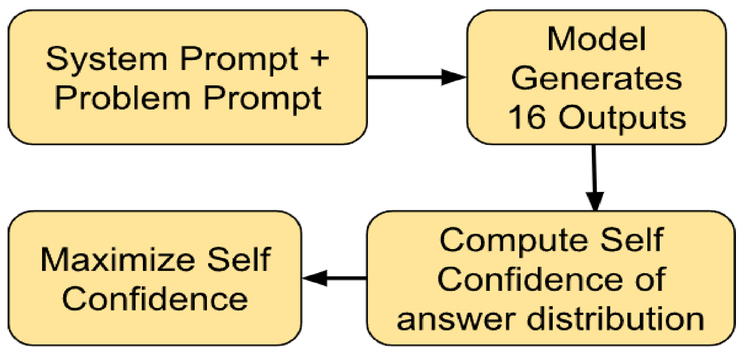

Fig. 1 Training Flow Diagram

Trained on **720 Verilog problems** from the Verithoughts database [2] with **16 generations per prompt**, the model learns to generalize to unseen Verilog tasks despite limited data.

Results

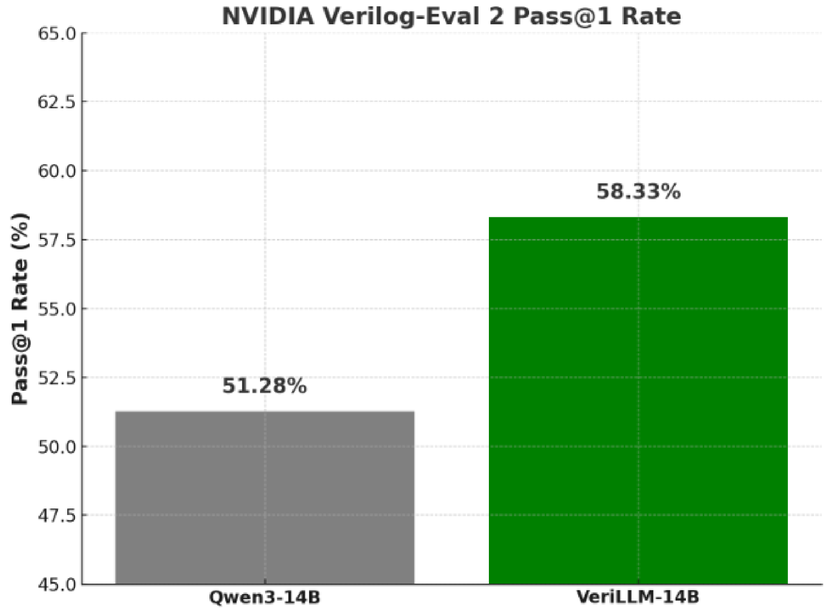

Fig. 2 Verilog-Eval Pass Rate

The baseline **QWEN3-14B model** achieved **a 51.28% pass rate** on **Verilog-Eval2**. After self-reward fine-tuning, **VeriLLM** improved to a **58.33% pass rate**, a **7.05% enhancement**, demonstrating the efficacy of the **Intuitor** approach in adapting to Verilog tasks.

The fine-tuned **VeriLLM** also demonstrated **more advanced reasoning techniques naturally overtime**. The self confidence evaluation (shown right) also quickly peaks and then collapses, demonstrating specific parameters.

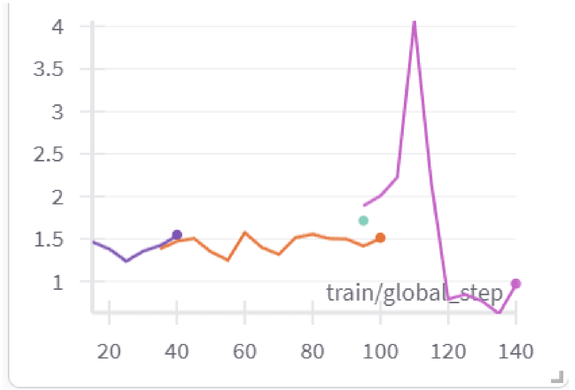

Fig. 3 Self-Confidence over step interval

Conclusion & Future Work

VeriLLM's self-reward training boosts Verilog-LLM performance, confirming Intuitor's value in data-scarce domains. **Future work aims to improve pass rates by 15%**, explore AI-generated prompts for complex tasks (e.g., **NVIDIA's RTL eval**), and integrate **VeriLLM** into agentic hardware design tools for streamlined workflows.

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References:
[1] *Learning to Reason without External Rewards*, arXiv:2505.19590, 2025.
[2] VeriThoughts: Enabling Automated Verilog Code Generation using Reasoning and Formal Verification, arXiv:2505.20302, 2025.

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