Enhancing Thermal Management and Reliability in Fan-Out Wafer-Level Packaging

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Motivation

The increasing demand for high-performance and compact electronic devices necessitates continuous innovations in semiconductor packaging technologies. Fan-Out Wafer-Level Packaging (FOWLP) has emerged as a promising solution. However, there are inherent limitations of FOWLP, particularly in thermal management and reliability. This research project explores the effects of adding Through Mold Vias (TMVs) made from copper to improve the packages thermal performance.

To the right, the top view (Fig. a) and cross-sectional view (Fig. b) of a conventional FOWLP design is shown. With the Chip (red) in the center, surrounded by the Mold Compound and the Copper redistribution layer (light green). Then the solder balls connect that layer with the circuit board, allowing the chip to communicate with the device.

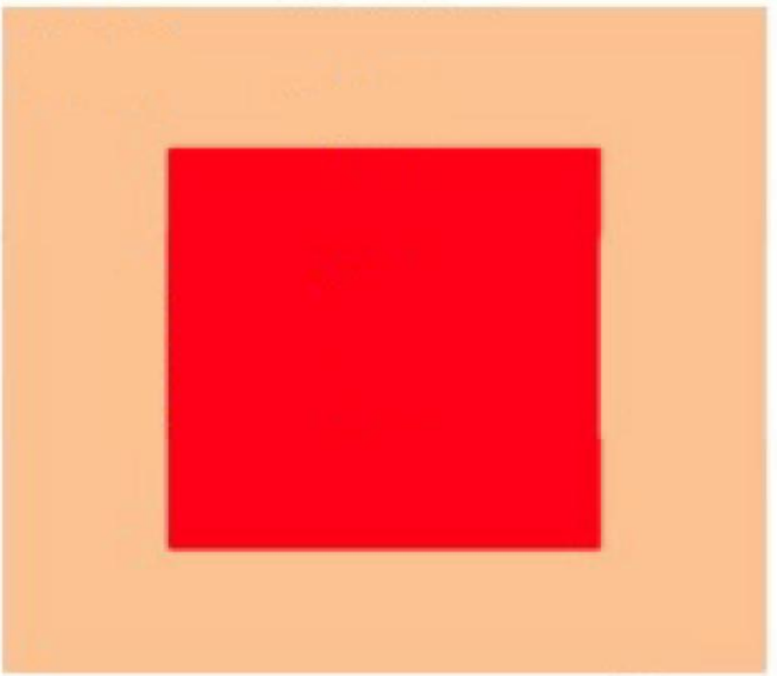

Fig. a

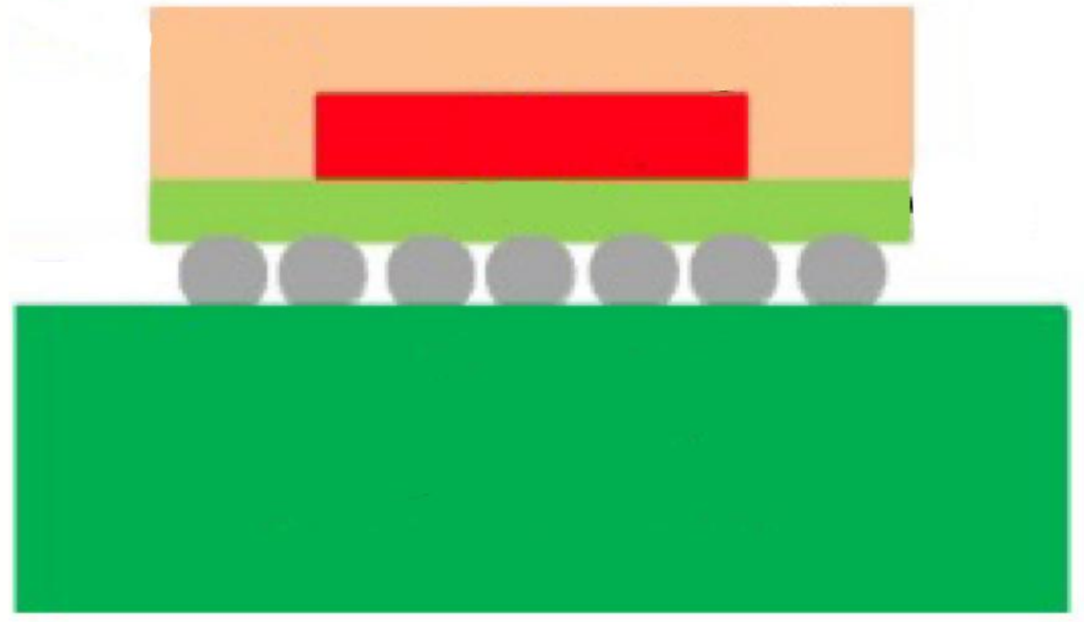

Fig. b

Our Goal

Create a realistic model of the FOWLP as well as a matching model with the TMVs. Then run a thermal stress simulation to see how the different models compare. Finally quantify the results to show a theoretical improvement as a result of the TMVs.

Progress & Challenges

Both models were created to scale and with accurate material properties. The Mold Compound with TMVs (fig. c) is shown using a 10x10 grid of copper vias. The entire model (fig d.) is shown including the heat sink on the back and excluding the circuit board for visibility. After the model were created, they could not be simulated due to limitations within the software and the complexity of the model. A more advanced license of Ansys Mechanical APDL is required to properly simulate the model.

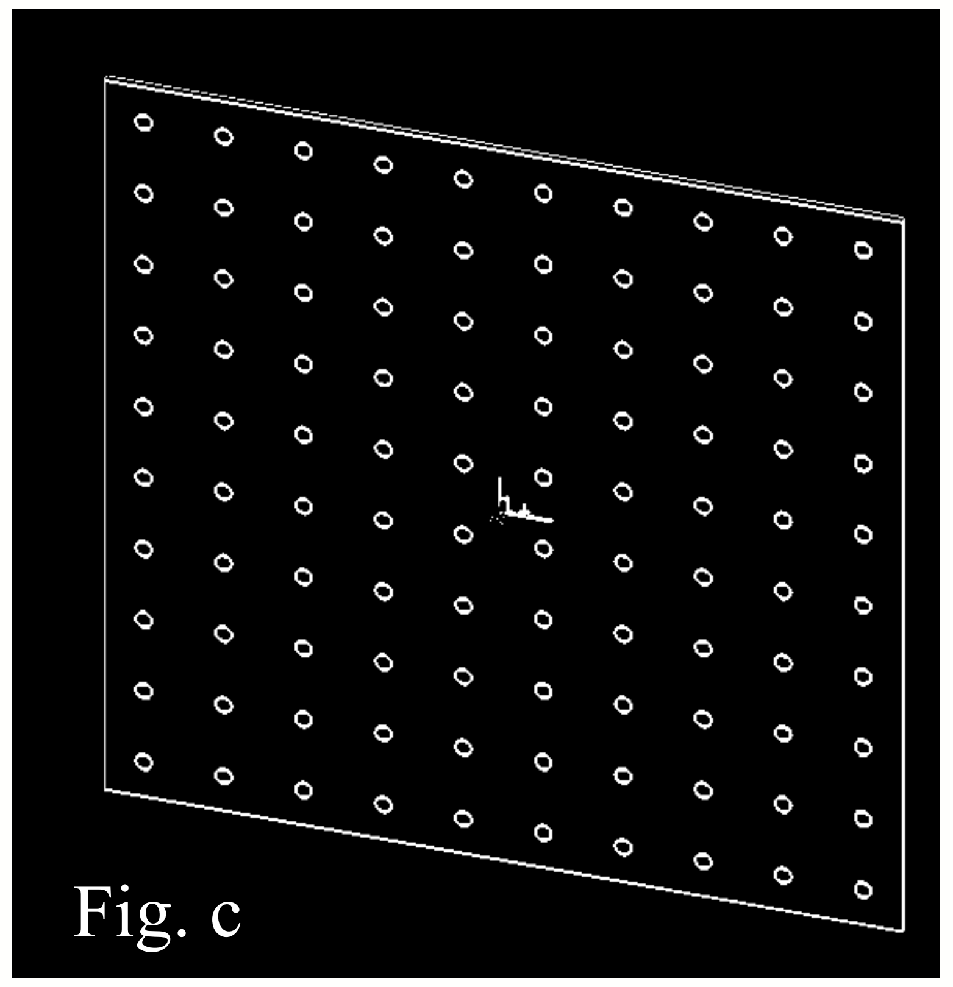

Fig. c

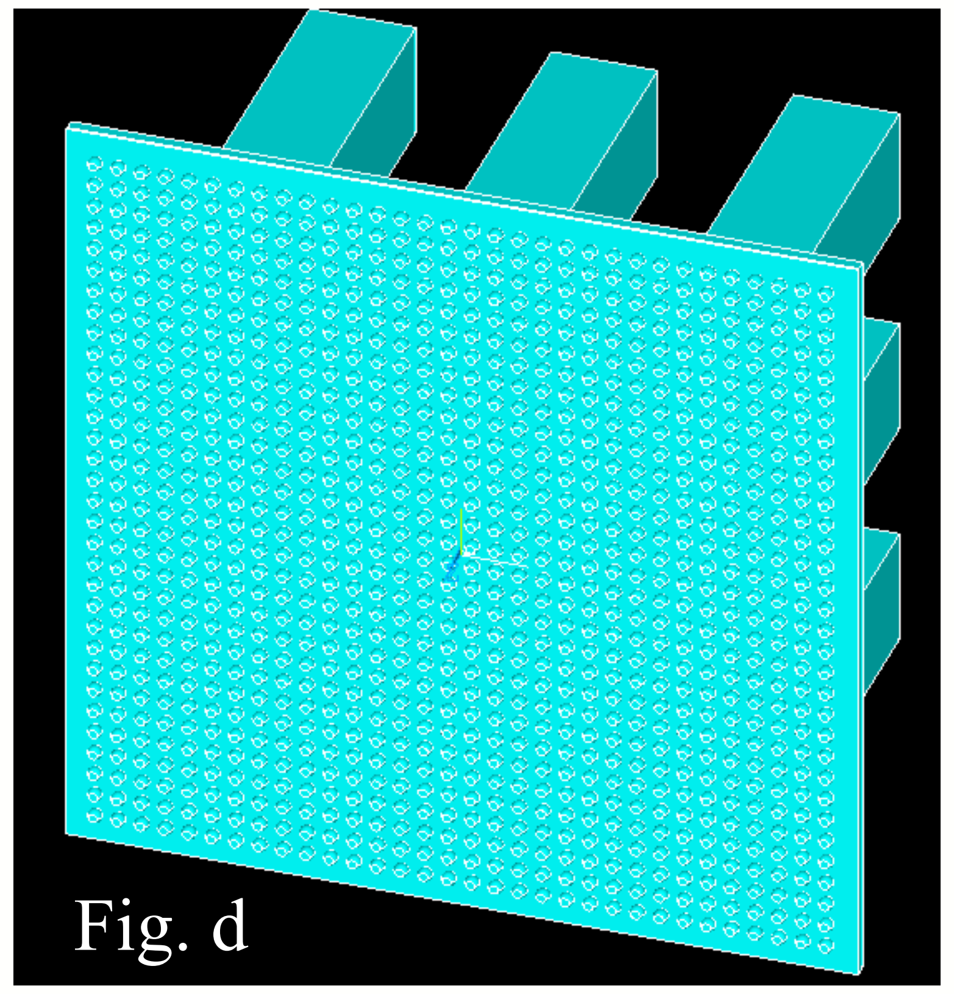

Fig. d

The Model

The models were created using Ansys Mechanical APDL. The model consisted of a Silicon Chip$_{(10x10x0.1mm)}$ embedded in a ceramic mold compound$_{(13.4x13.4x0.2mm)}$. 3 copper redistribution layers$_{(13.4x13.4x0.04mm)}$ (RDLs) interacted with the chip and connected it with the 32x32 solder ball grid array. Each solder ball was 0.25mm in diameter and had a pitch of 0.4mm. Lastly an aluminum heat sink was added to the back of the package and the circuit board was attached to the solder balls. An isometric cross sectional view of the model is shown (fig. e).

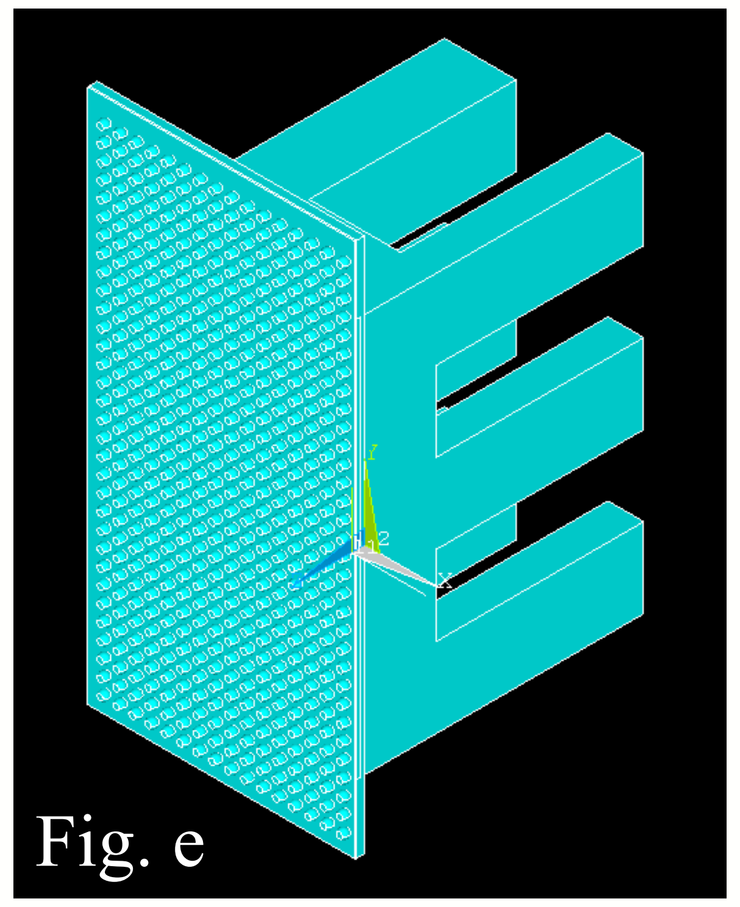

Fig. e

Future Work

Obtain advanced licensure to run iterative thermal and structural simulations optimizing the TMV method for performance and manufacturing.

Acknowledgments

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