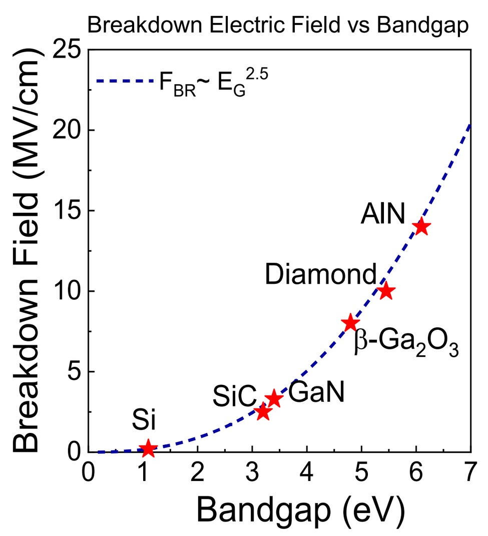
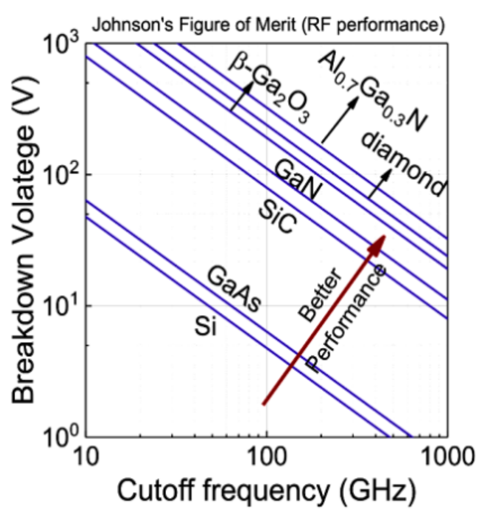
Diamond Static Induction Transistor Design and Optimization in TCAD

David M McComas, Electrical Engineering
Mentor: Dr. Nidhin Kurian Kalarickal, Assistant Professor,
School of Electrical, Computer and Energy Engineering, Arizona State University

Ultra-wide Bandgap (UWBG) Semiconductors for RF Devices

RF/mm-wave applications





Theoretical P_{out} of an RF transistor

$$P_{out} = \frac{\epsilon F_{BR}^2 v_{sat}^2}{64\pi} \frac{1}{\sqrt{G_p f}} \sqrt{\frac{R_{out}}{R_{in}}}$$

Theoretical PAE of an RF transistor

$$PAE = \frac{P_{out}^{RF} - P_{in}^{RF}}{P_{in}^{DC}}$$

- UWBG semiconductors offer high breakdown fields (F_{BR}) and saturation velocity (v_{sat}).
- Johnson's figure of merit (JFOM) for RF devices, $V_{BR} \times f_T = F_{BR} \times v_{sat}/2\pi$, predicts RF performance
- Enables achieving high power density (P_{out}), gain (G_P) and power added efficiency (PAE).

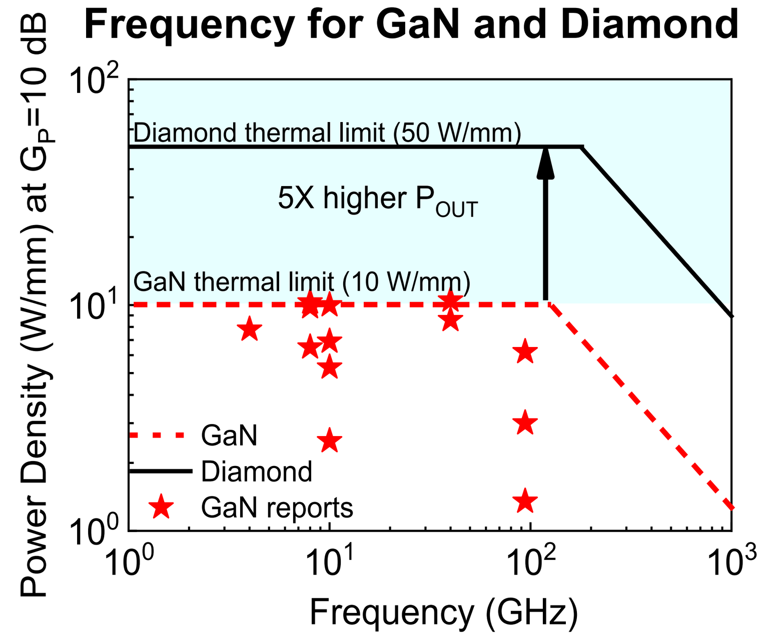
The Diamond Advantage

Semiconductor Properties

		Si	4H-SiC	GaN	Ga_2O_3	Diamond
Bandgap E_G [eV]		1.10	3.20	3.45	4.9	5.47
Saturation drift velocity v_S [x 10^7 cm/s]	Electron	1.1	1.9	2.5	2	2.5, *1.9* [5]
	Hole	0.8	1.2	–	–	1.0, *1.4* [5], *0.6* [6]
Carrier mobility μ [cm^2/Vs]	Electron	1500	1000	1500	300	*4500* [1],
	Hole	450	120	200	–	*3800* [1], *2000* [7]
Breakdown field E_{max} [MV/cm]		0.3	2.8	5	8	10–22, *9.5* [8]
Dielectric constant ε_r		11.9	9.66	8.9	9.93	5.7
Thermal conductivity λ [W/mK]		150	490	130	23	2200

H. Umezawa, "Recent advances in diamond power semiconductor devices," Materials Science in Semiconductor Processing, vol. 78, pp. 147–156, 2018

Theoretical power density vs Frequency for GaN and Diamond

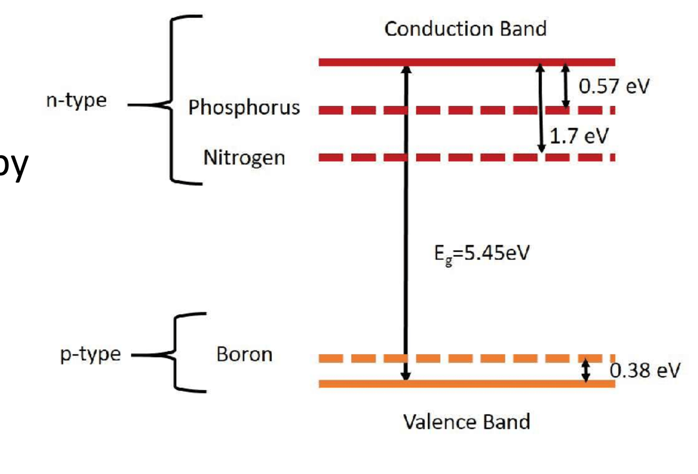


- Diamond's semiconductor properties are ideal for high power RF devices, as indicated by JFOM.
- Power density of GaN HEMTs on SiC (state of the art RF transistor) is limited to 10 W/mm due to thermal conductivity of SiC substrate.

Diamond Static Induction Transistor

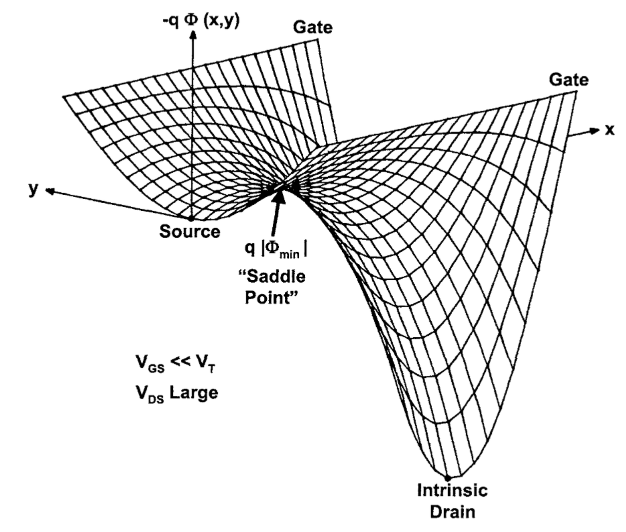
- Key limitation in diamond: **Deep donors and acceptors** limit current density in diamond devices by trapping carriers.
- **Static Induction Transistors (SITs)** address this limitation by enabling **space charge limited conduction** allowing for injection of carriers directly from the source contact.
- ($J_{SCLC} = \frac{9}{8}\frac{\epsilon \mu V^2}{L^3}$)
- The diamond SIT is a vertical p-type normally-on FET → a positive bias must be applied to the gate to stop current flow via drain-induced barrier lowering (DIBL)

Diamond band diagram with dopant ionization energy (eV)



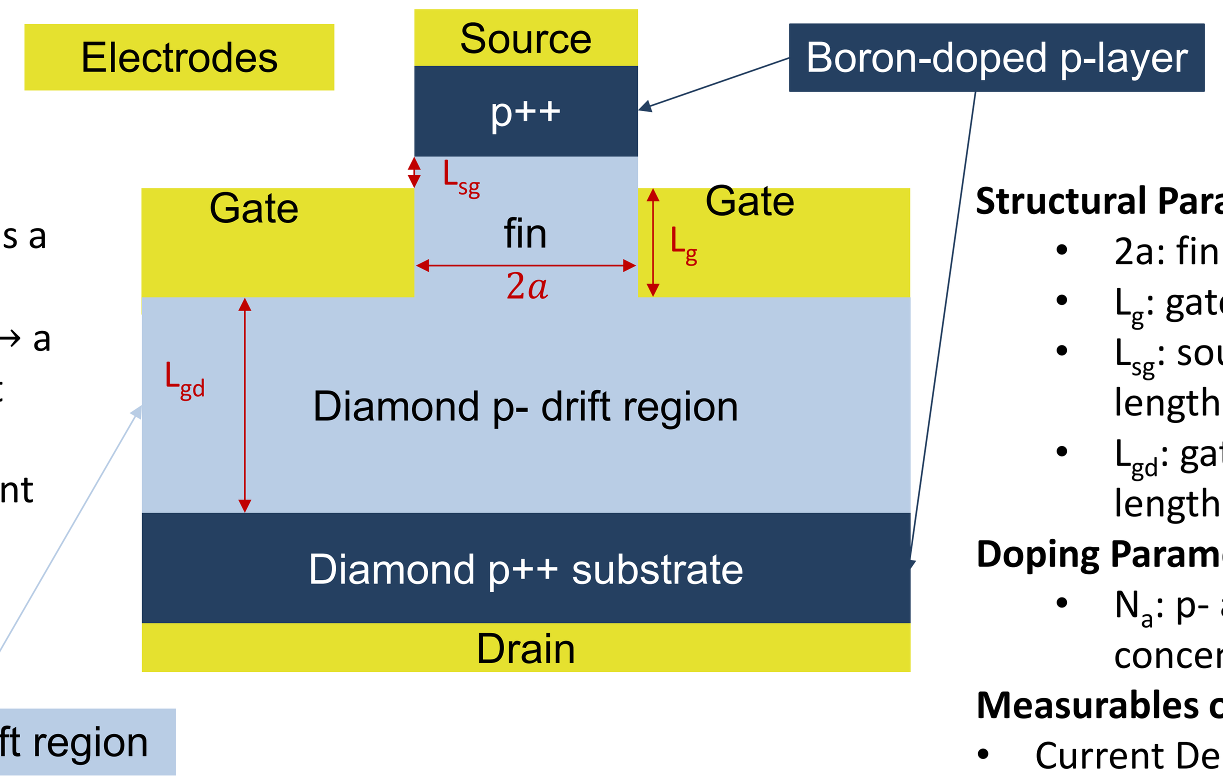
J. Letellier, "Diamond Schottky diodes improvement to pave the way to high power electronic application," phdthesis, 2019

SCLC Potential Map



Gregory C. Desalvo. "SILICON CARBIDE STATIC INDUCTION TRANSISTORS," in *International Journal of High Speed Electronics and Systems*, vol. 15, pp. 997-1033, 2005.

Schematic of diamond SIT



Structural Parameters

- 2a: fin width
- L_g: gate length
- L_{sg}: source-gate length
- L_{gd}: gate-drain length

Doping Parameter

- N_a: p- acceptor concentration

Measurables of Interest:

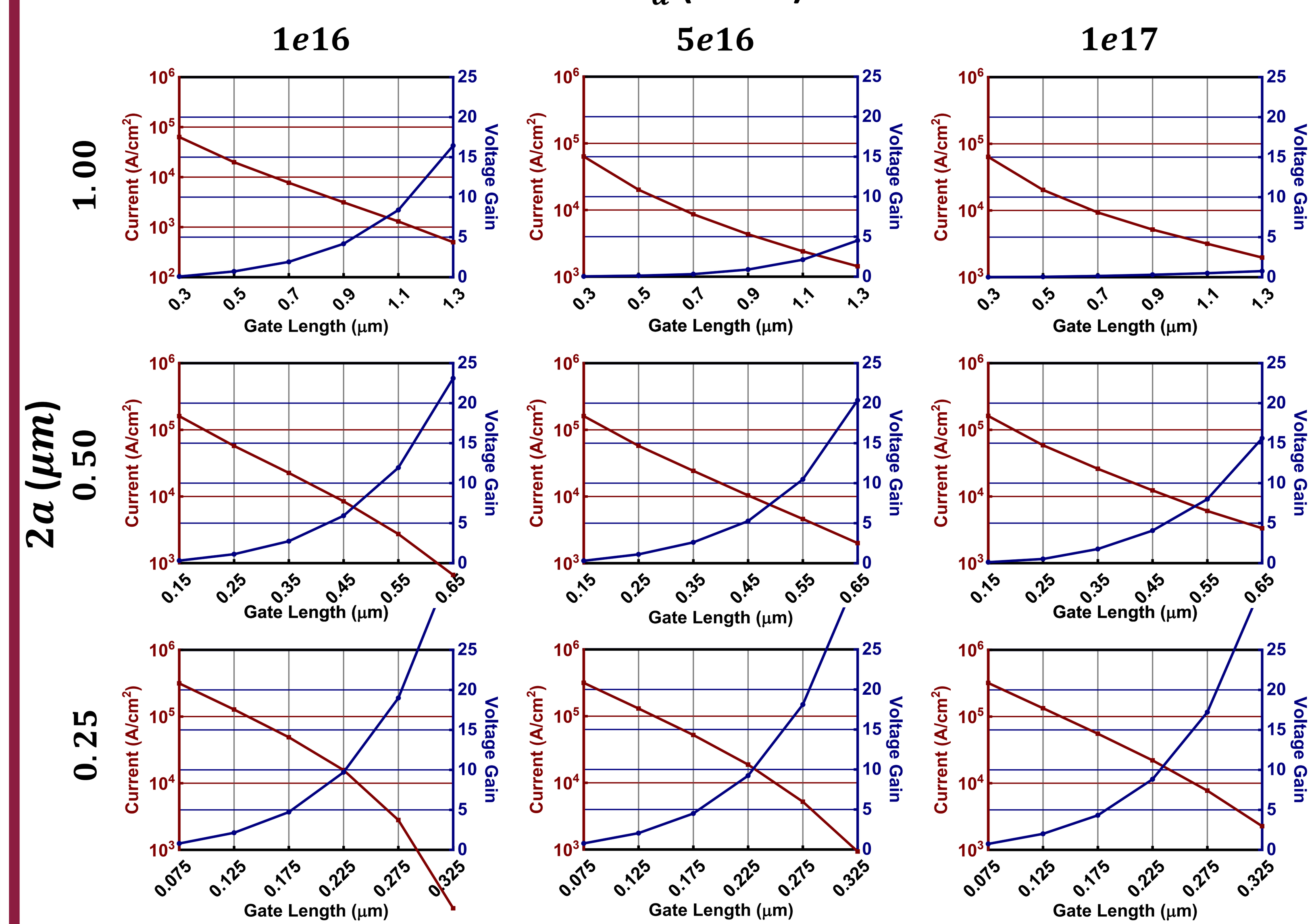
- Current Density, J
- Gain, G_p
- Output Power, P_{out}
- Power Added Efficiency, PAE
- Transconductance, g_m
- Drain Threshold Voltage, V_{th}
- On-resistance, R_{on}
- Breakdown Voltage, V_{br}
- Cut-off Frequency, f_c
- Device capacitances

- **2a & L_g: fin width & gate length**
  - Controls the gate's ability to pinch off the channel
  - High a and low L_g yields high J, but makes it difficult to turn off (low μ)
  - Low a and high L_g yields low J and it is difficult to turn on (high μ)
- **L_{sg}: source-gate length**
  - Low leakage path with sufficient V_{BR} must exist between gate and source
  - Small L_{sg} minimizes R_{source}
  - μ increases as L_{sg} increases for fixed L_g
- **L_{gd}: gate-drain length**
  - Determined by two conflicting requirements of low R_{drain} and high V_{BR}
  - Must be tailored to each doping
  - μ increases and f_c decreases as L_{gd} increases
- **N_a: acceptor concentration**
  - μ decreases and J increases as N_a increases
- TCAD simulations map the parameter space to applications and reveal desirable device structures

DC Results

The voltage gain and output current are metrics of RF amplifier performance. Voltage gain is also used to calculate the output resistance. Target μ=10-15, target J=1-10 kA cm^{-2}

- **Aspect Ratio, AR** $= \frac{L_g}{a}$, plotted from 0.6 to 2.6 for all devices shown
- **Voltage Gain (Amplification Factor), μ**: Unitless factor that describes the ratio of change in the source-drain voltage to the change in gate voltage required to cause the same change in output current $\mu = \frac{\Delta V_d}{\Delta V_g} = \frac{V_{d\,2} - V_{d\,1}}{V_{g\,2} - V_{g\,1}}$
- **Transconductance, g_m**: The ratio of output current to the source-drain voltage
- **Output Current, J** (measurable) $J = 1e5\frac{V_d I}{n * 2a}\ (A\ cm^{-2})$
- **Output Resistance, R_{out}** $= \frac{\mu}{g_m}$, used to calculate P_{out}



- In this project, N_a was swept from 1e15-1e18 cm^{-3} and 2a was swept from 100 nm - 1.0 μm. Voltage gains and current densities from a sample of devices are shown.
- Note that the smaller devices have significantly larger J for any given μ.

Conclusion

- The device simulations show promise according to the metrics used in the study. However, it should be noted that smaller devices present a greater challenge in fabrication.
- The next steps for this project is to continue sweeping N_a to lower concentrations, expand the sweep to vary L_{gd} and L_{sg}, and begin simulating RF characteristics.
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FURI

Ira A. Fulton Schools of Engineering
Arizona State University