Conductive Filament Modeling and Reliability Prediction in Pt/SiO_x/TiN Resistive Random Access Memory

Andrew Rubio, Electrical Engineering
Mentor(s): Dr. Ying-Chen Daphne Chen, Assistant Professor
School of Electrical, Computer and Energy Engineering (ECEE), Arizona State University

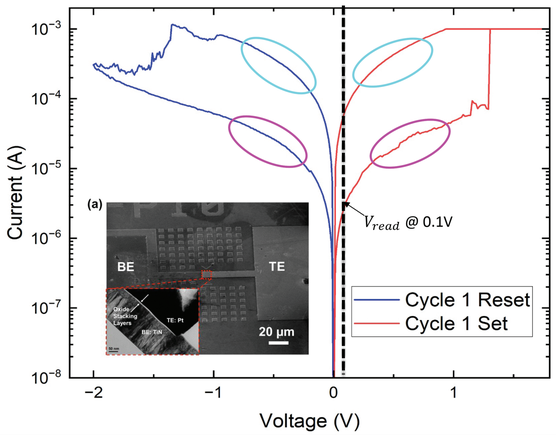
Motivation

Modern computing often uses the von Neumann architecture, where the power consumption between data transfer from memory to CPU causes a limitation on computing efficiency. Emerging memory technology has been proposed as the device to overcome this bottleneck, where their high-density storage memory and computational functions will be used towards AI and post CMOS era.

In this study: The resistive switching behaviors on Pt/SiO_x (11 nm)/TiN RRAM devices were fabricated by RF sputtering and characterized with device area dependency of 0.4, 0.6, 0.8, and 1 μm.

Background

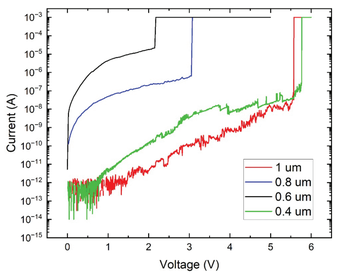
- Oxide-based ReRAM switches between high and low resistance states under forward or reverse bias.
- Switching occurs due to a conductive filament that is formed and ruptured with SET and RESET, respectively. LRS and HRS indicates a digital 1 or 0 on a non-volatile memory application.



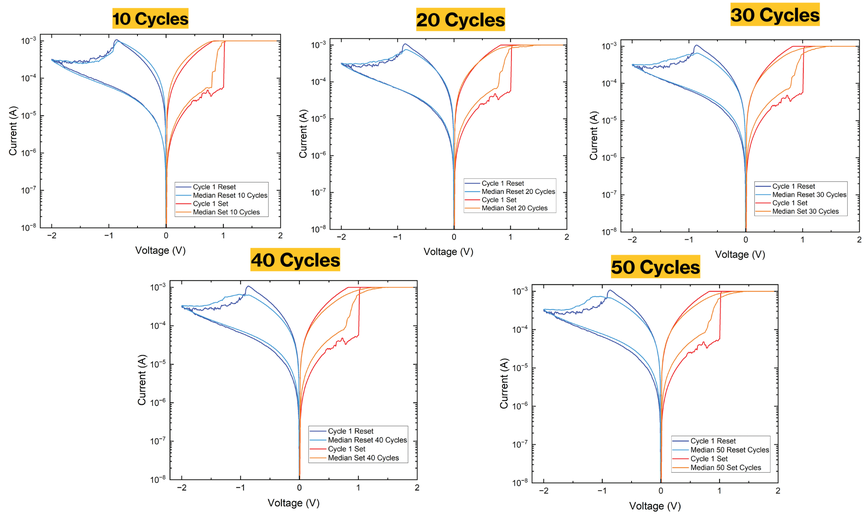
A memory window can be observed through the difference in HRS and LRS. The large window correlates to a larger readability between ON and OFF.

Methods

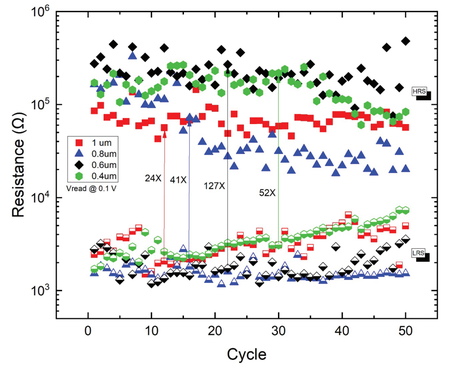
- A current compliance limit (CCL) of 1 mA, SET voltage of 3V, and a RESET voltage of -2V were set all throughout SET and electroforming processes to prevent the dielectric permanent breakdown.
- The electroforming voltage is modulated along with stress forming as if not an electroformation has been observed (5V – 8V).
- A FormFactor S200 probe station was used for device characterization

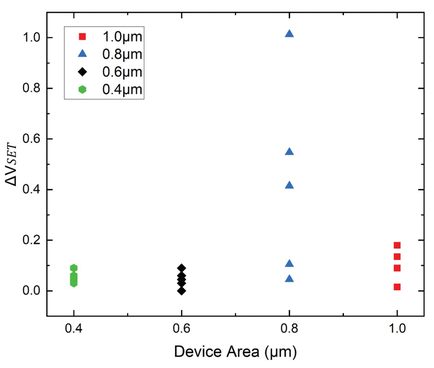


Device Variation



Results and Future Work





- DC endurance shows good memory windows (>10) for various device sizes. The device of 0.6 μm shows notable set voltage(> 200 mV) variation after cycling.
- To study the correlation between **variations of V_{SET}** and MW closure, pulse testing will be conducted on Pt/SiO_x/TiN RRAM. Linear fitting of the I-V curves will be conducted to better understand conductive filamentary switching mechanisms throughout the SET and RESET process during reliability testing.

Conclusion

- **The SiO_x-based RRAM with device area dependency has been studied for high density storage, new computing, and CMOS compatible BEOL integration.**
- **Pt/SiO_x/TiN devices of area 0.6 μm show a large memory window (>100), great DC endurance cycles, less MW closure, and low operation voltage variation.**
- **The memory window closure as a function of area dependency and variation of operational voltage will be further studied.**

FURI

SDRL Semiconductors and Device Research Lab

tsmc

Ira A. Fulton Schools of Engineering
Arizona State University