Diamond Static Induction Transistors

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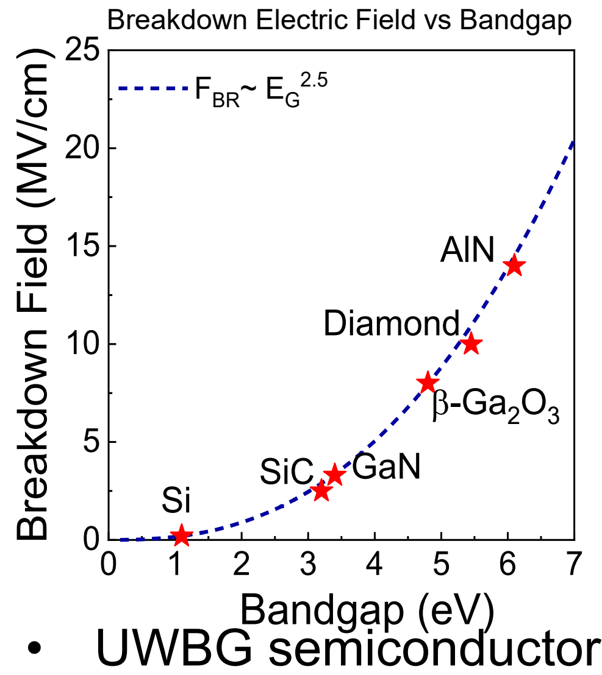
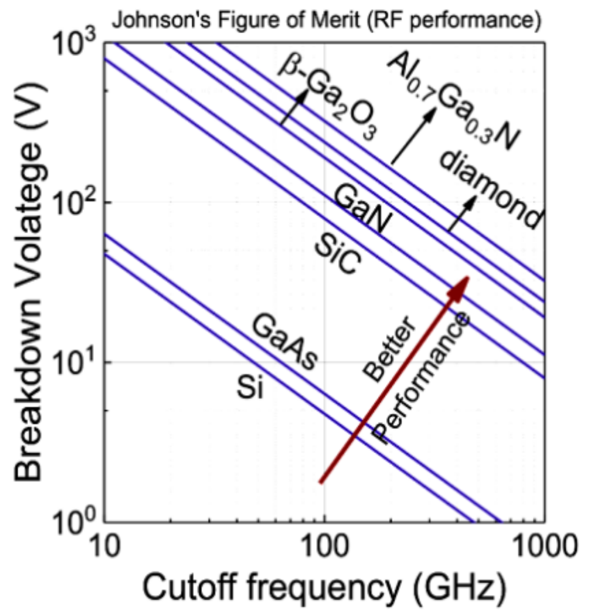
Ultra-wide Bandgap (UWBG) Semiconductors for RF Devices





Theoretical P_{out} of an RF transistor

$$P_{out} = \frac{\epsilon F_{BR}^2 v_{sat}^2}{64\pi} \frac{1}{\sqrt{G_p f}} \sqrt{\frac{R_{out}}{R_{in}}}$$

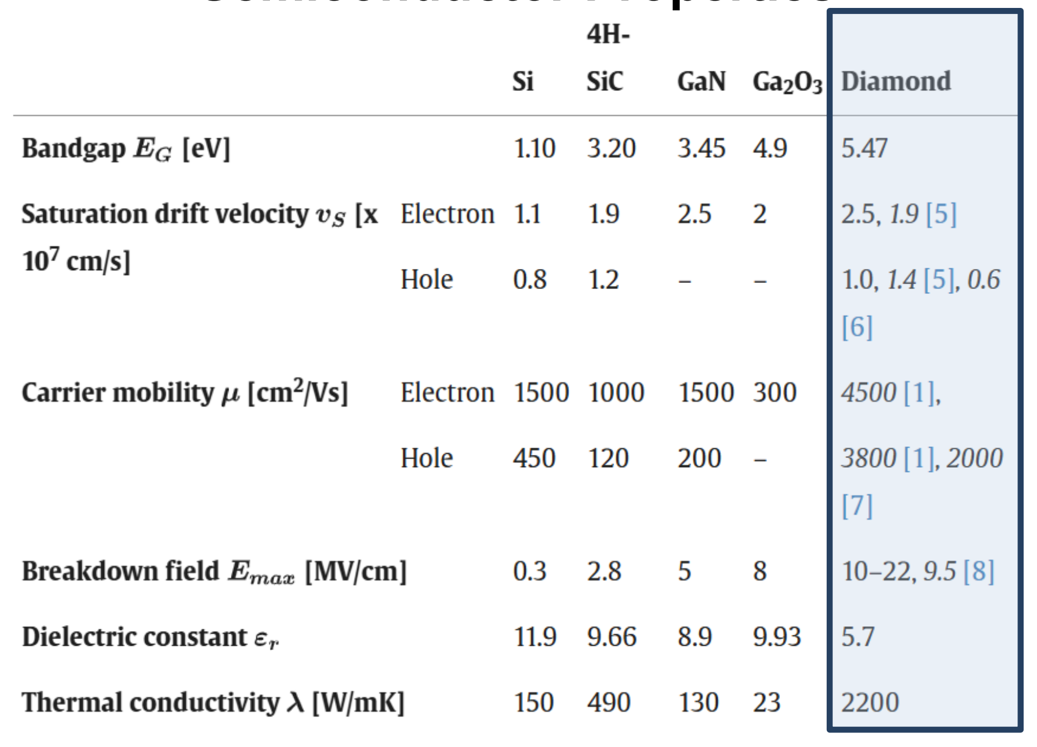
Theoretical PAE of an RF transistor

$$PAE = \frac{P_{out}^{RF} - P_{in}^{RF}}{P_{in}^{DC}}$$

- UWBG semiconductors offer high breakdown fields (F_{BR}) and saturation velocity (v_{sat}).
- Johnson's figure of merit (JFOM) for RF devices, $\boldsymbol{V_{BR} \times f_T = F_{BR} \times v_{sat}/2\pi}$, predicts RF performance
- Enables achieving high power density (P_{out}), gain (G_P) and power added efficiency (PAE).

The Diamond Advantage

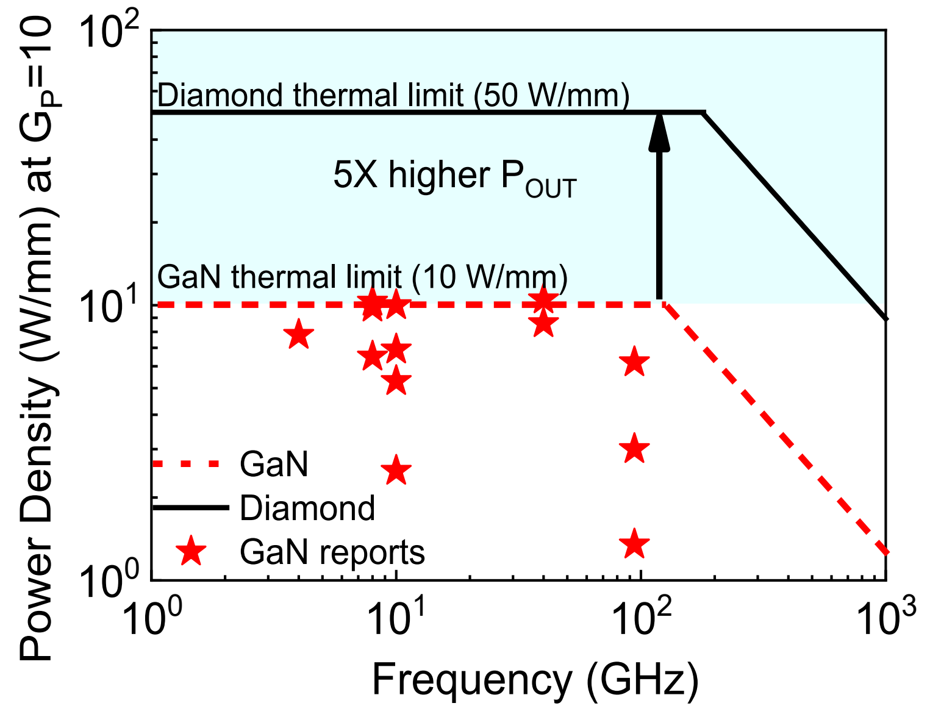
Semiconductor Properties



		Si	4H-SiC	GaN	Ga$_2$O$_3$	Diamond
Bandgap E_G [eV]		1.10	3.20	3.45	4.9	5.47
Saturation drift velocity v_S [x 10^7 cm/s]	Electron	1.1	1.9	2.5	2	2.5, *1.9* [5]
	Hole	0.8	1.2	–	–	1.0, *1.4* [5], *0.6* [6]
Carrier mobility μ [cm^2/Vs]	Electron	1500	1000	1500	300	*4500* [1],
	Hole	450	120	200	–	*3800* [1], *2000* [7]
Breakdown field E_{max} [MV/cm]		0.3	2.8	5	8	10–22, *9.5* [8]
Dielectric constant ε_r		11.9	9.66	8.9	9.93	5.7
Thermal conductivity λ [W/mK]		150	490	130	23	2200

H. Umezawa, "Recent advances in diamond power semiconductor devices," Materials Science in Semiconductor Processing, vol. 78, pp. 147–156, 2018

Theoretical power density vs Frequency for GaN and Diamond

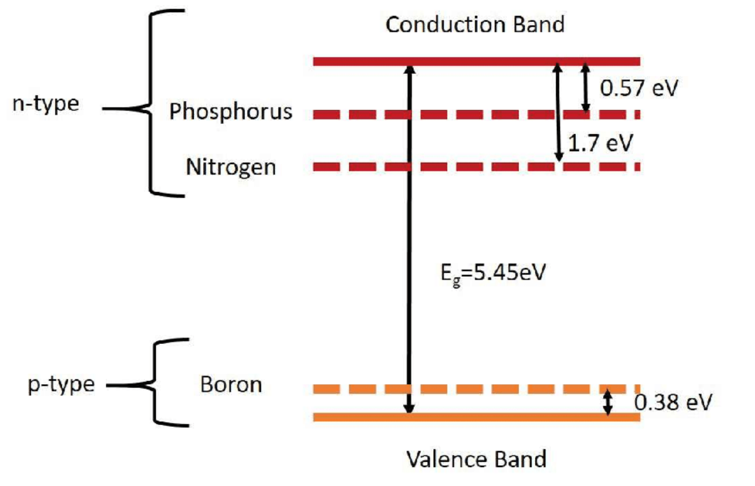


- Diamond's semiconductor properties are ideal for high power RF devices, as indicated by JFOM.
- Power density of GaN HEMTs on SiC (state of the art RF transistor) is limited to 10 W/mm due to thermal conductivity of SiC substrate.

Diamond Static Induction Transistor

- Key limitation in diamond: **Deep donors and acceptors** limit current density in diamond devices by trapping carriers.
- **Static Induction Transistors (SITs)** address this limitation by enabling space charge limited conduction ($\boldsymbol{J_{SCLC}}$= $\frac{9}{8}\frac{\epsilon\mu V^2}{L^3}$) allowing for injection of carriers directly from the source contact.
- Space charge limited conduction is effective in diamond for breakdown voltages of ~100 V as shown in Baligas's FOM (BFOM) with J_{SCLC}.

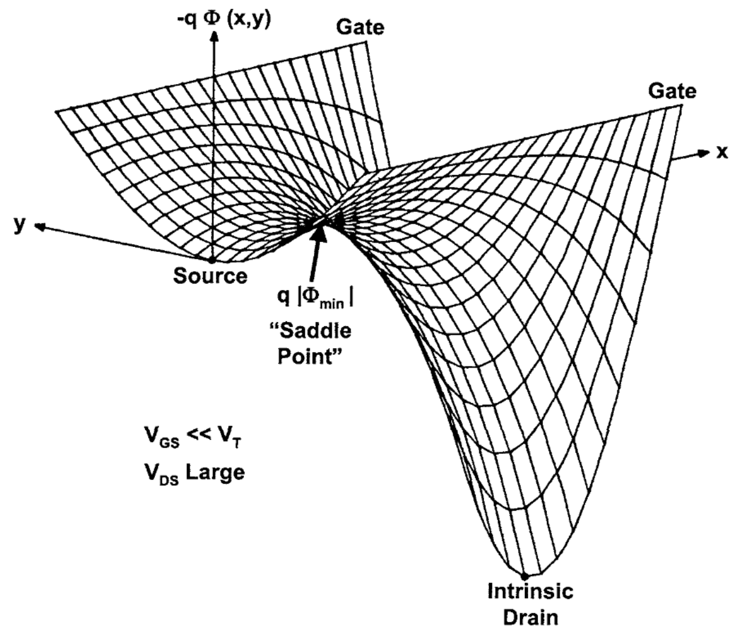
Diamond band diagram with dopant ionization energy (eV)



J. Letellier, "Diamond Schottky diodes improvement to pave the way to high power electronic application," phdthesis, 2019

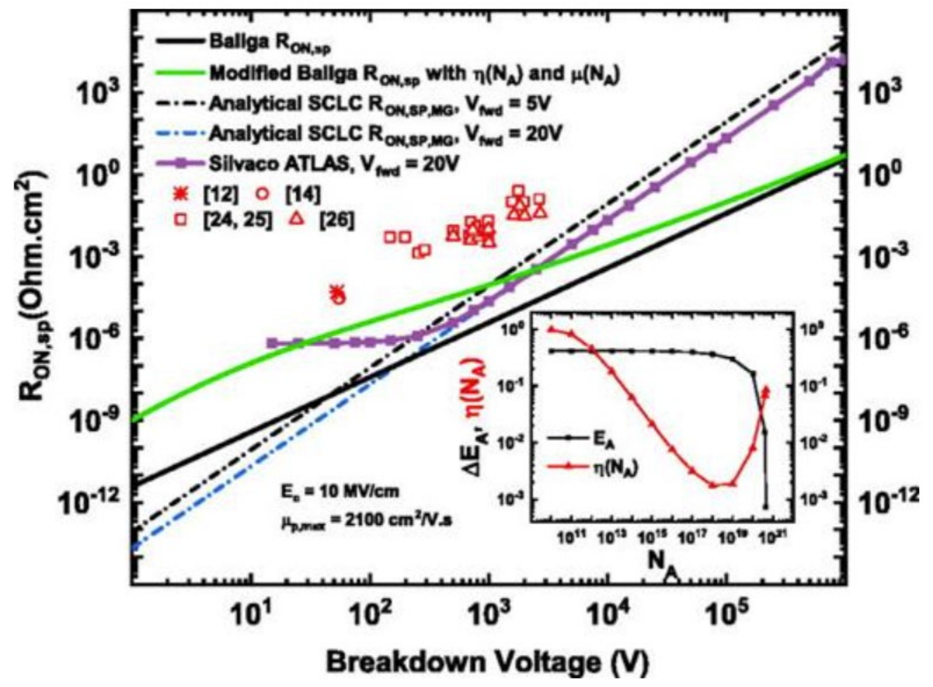
SCLC Potential Map

- SCLC occurs in the SIT's triode-like mode due to static induction, also called drain-induced barrier lowering (DIBL).
- DIBL can be controlled during operation and in the design stage.



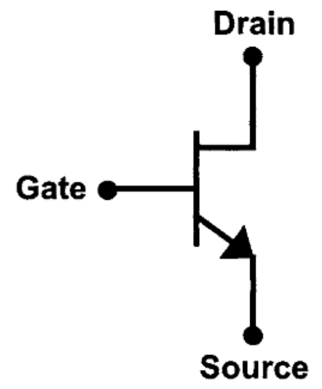
Gregory C. Desalvo. "SILICON CARBIDE STATIC INDUCTION TRANSISTORS," in *International Journal of High Speed Electronics and Systems*, vol. 15, pp. 997-1033, 2005.

BFOM with J_{SCLC}



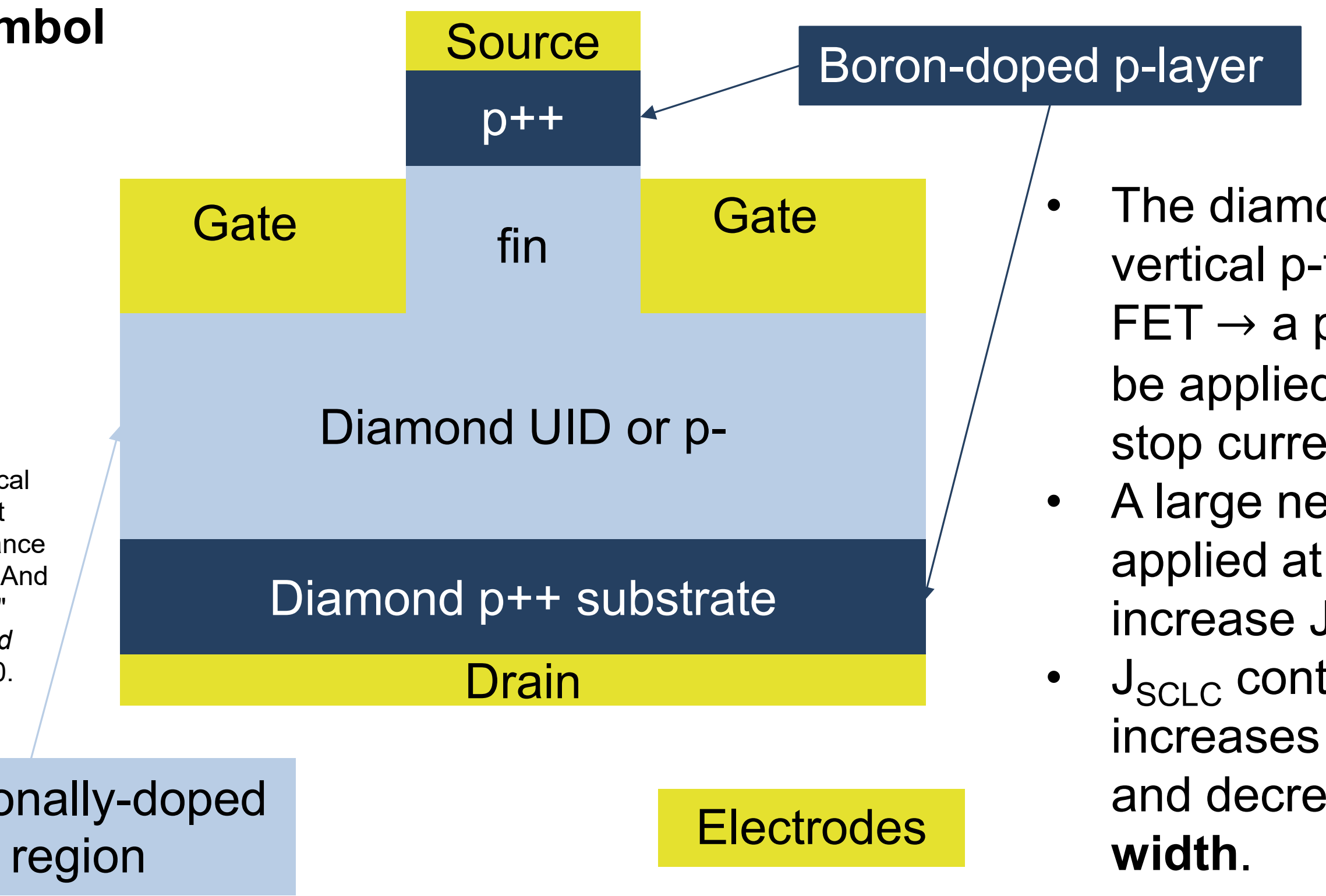
Kok Wai Lee, Yee Sin Ang, *Appl. Phys. Lett.* 2 October 2023; 123 (14)

SIT device symbol



Sung, YunMo, "Critical Analysis Of Sic Sit Design And Performance Based Upon Material And Device Properties" (2005). *Theses and Dissertations*. 1220.

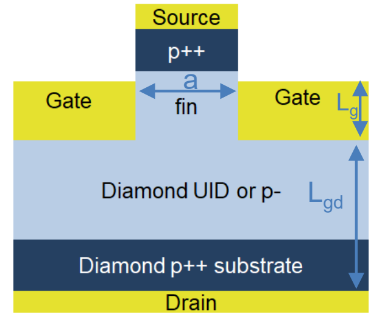
Schematic of diamond SIT



- The diamond SIT is a vertical p-type normally-on FET → a positive bias must be applied to the gate to stop current flow via DIBL.
- A large negative bias can be applied at the drain to increase J_{SCLC}.
- J_{SCLC} control strength increases with **gate length** and decreases with **fin width**.

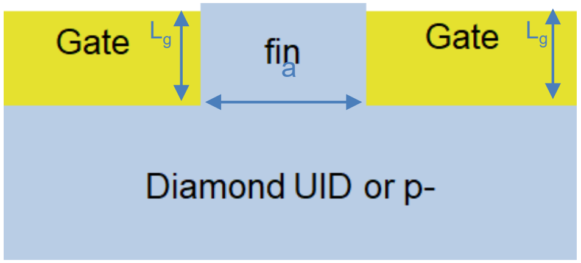
- Increasing the device length increases the breakdown voltage but decreases the cutoff frequency, while varying doping concentrations varies current density and switching speed.
- TCAD simulations map the parameter space to applications → find desirable parameter sets.
- Process development aims to create processes to fabricate SITs with desired parameters.

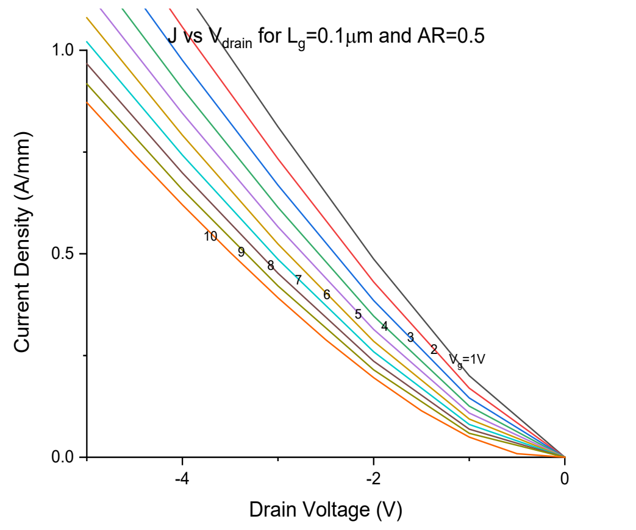
Fin Simulation and Fabrication

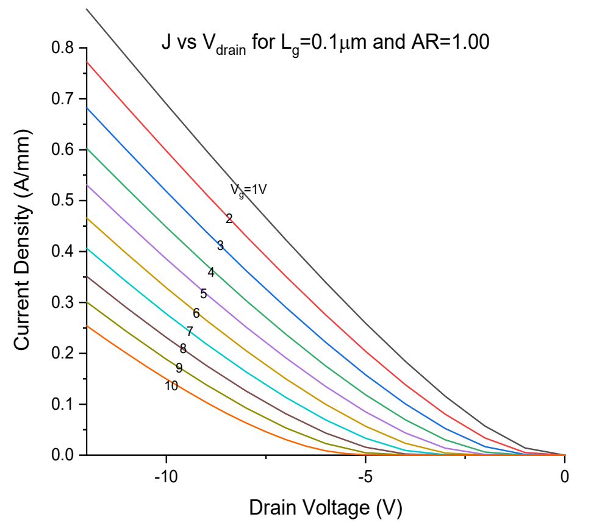


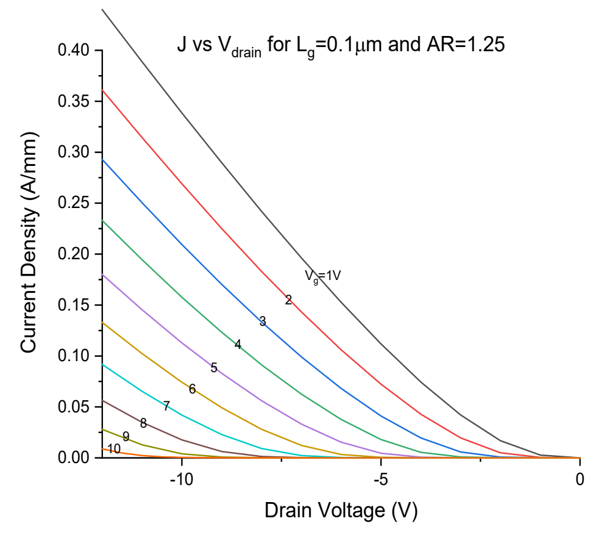
Aspect Ratio

$$AR = 2\left(\frac{L_g}{a}\right)$$

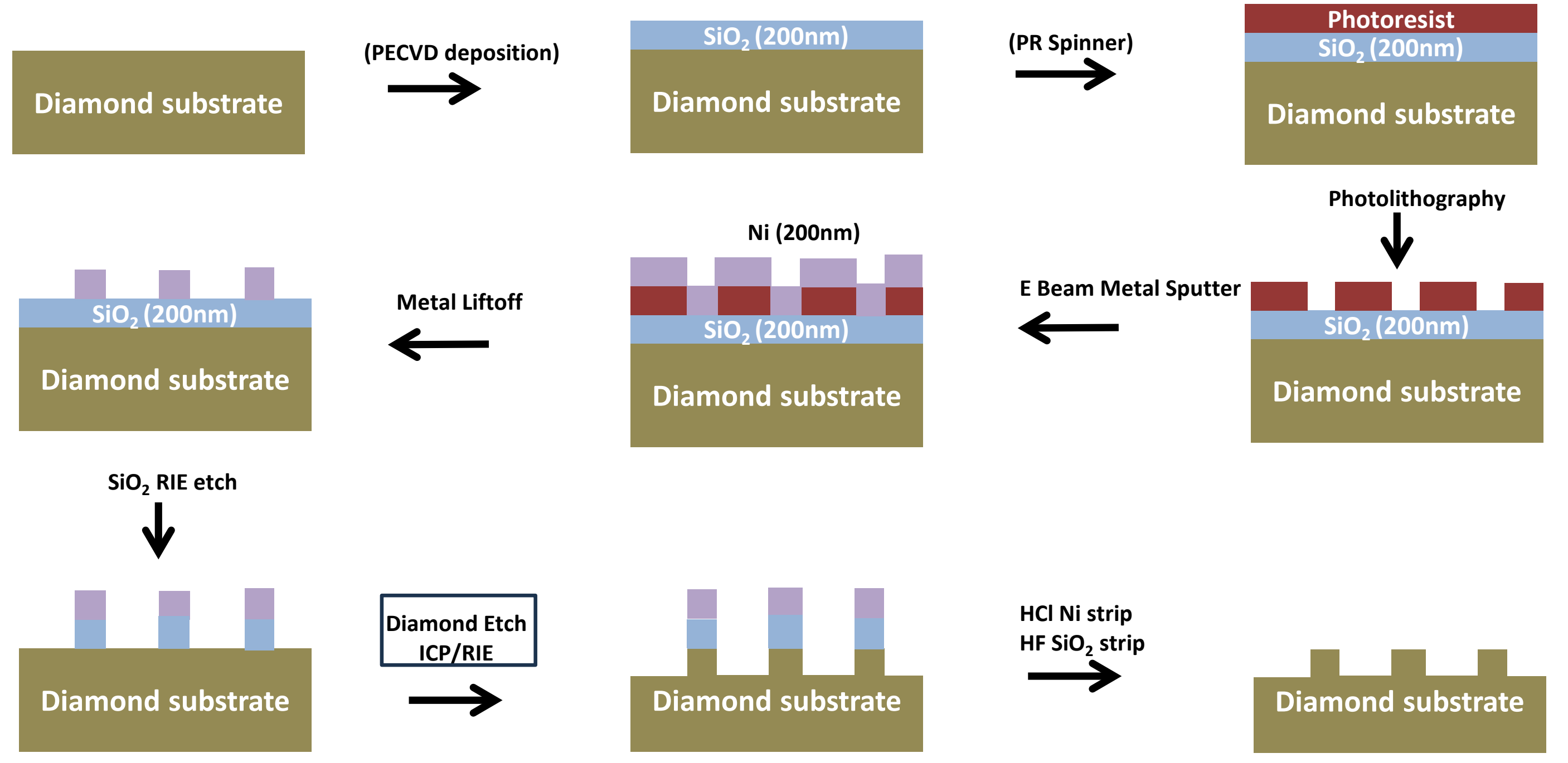






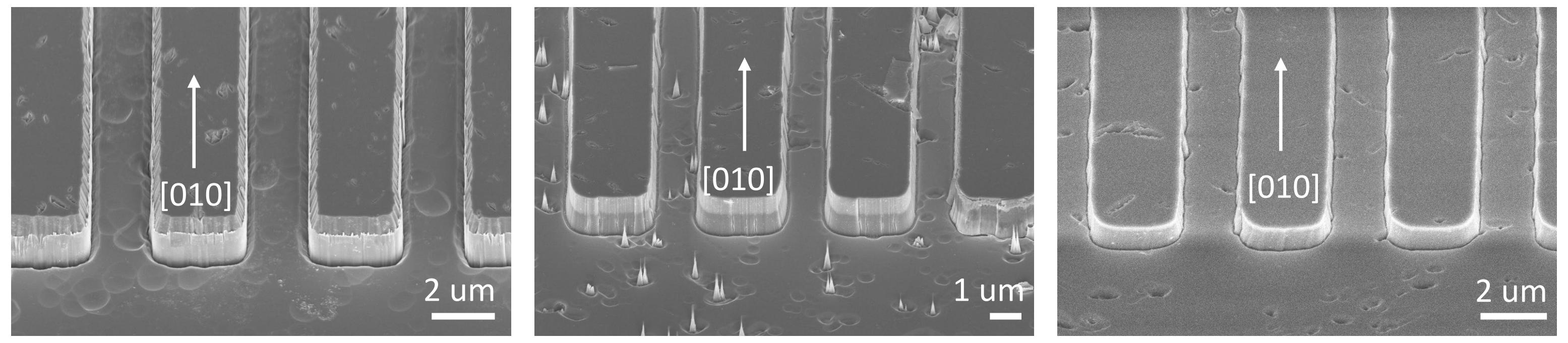


Etching Process Flow



Process design credit to Nabasindhu Das, PhD candidate, ASU ECEE

Tilted SEM of three etch recipes for [010] fins on (001) Diamond Substrate



Recipe credit to Nabasindhu Das, PhD candidate, ASU ECEE

Conclusion

- Increasing the fin aspect ratio lowers the current density and increases the magnitude turn-on voltage at the drain.
- The next steps for this project are to continue the parameter sweep with the source-gate length and doping profile, continue process development, and simulate thermal and ionizing radiation effects using FEA.

FURI

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