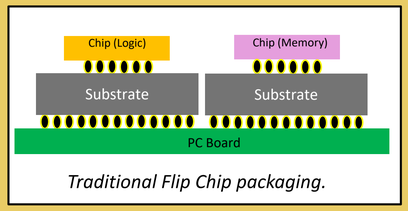
Thermal Management for 3D Heterogenous Integration of Semiconductor Packaging

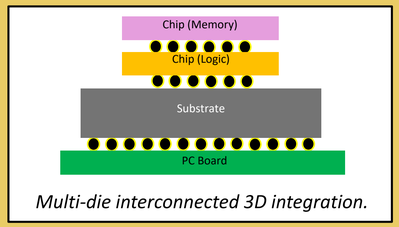
Rohit Mahavir Gandhi, Mechanical Engineering
Mentor: Robert Y. Wang, Associate Professor
School for Engineering of Matter, Transport and Energy

Motivation

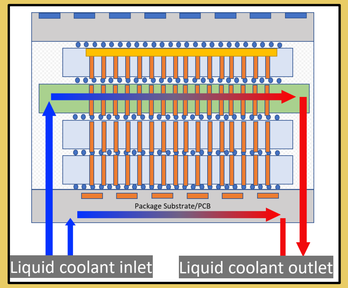
- 3D Heterogenous Integration of semiconductor devices provides performance advantages but comes with additional thermal challenges.



Traditional Flip Chip packaging.



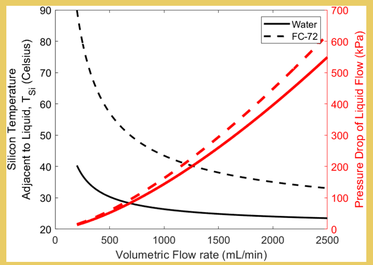
Multi-die interconnected 3D integration.

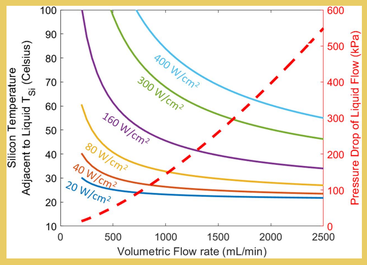


- A new class of thermal management system needs to be explored for 3D Packaging and intralayer microfluid cooling is a promising solution.

Analytical correlation-based analysis

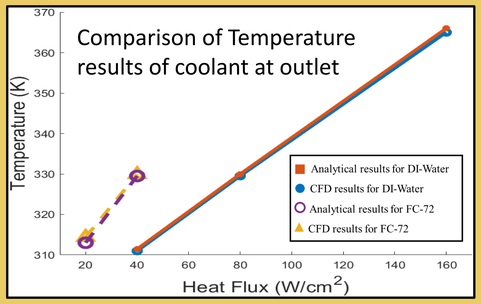
- Selecting an appropriate intralayer thermal management layer requires a systematic calculation process. By employing analytical correlations, we calculate the output temperature and pressure drop under various geometric parameters and power load conditions.
- We utilize two distinct coolants, DI-Water and FC-72, for the thermal performance and how variations in heat flux conditions affect chip temperature and fluidic pressure drop.

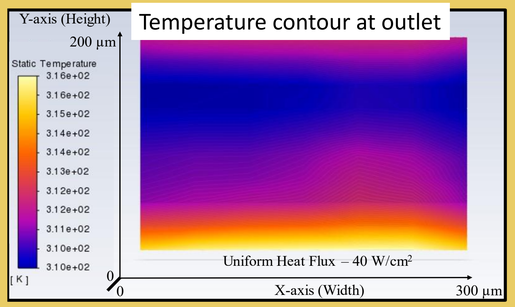


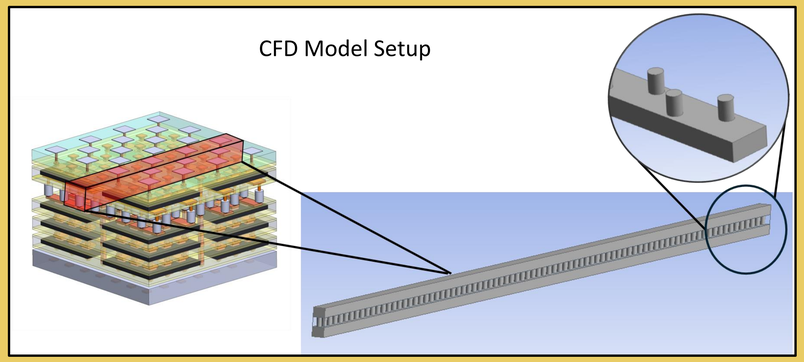


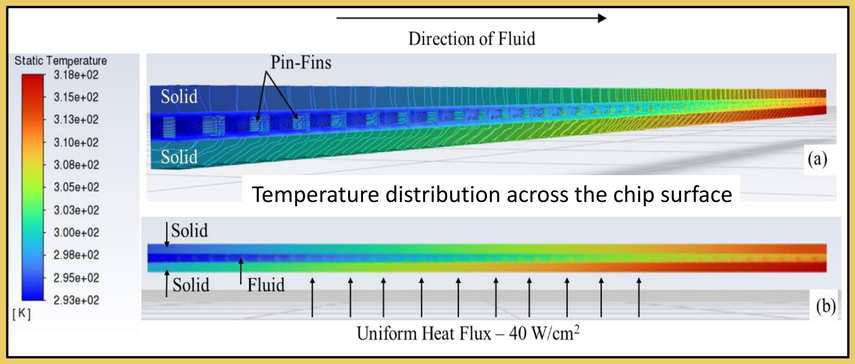
CFD Analysis.

- To understand the temperature distribution a computational fluid dynamics (CFD) analysis was carried out to examine optimal operating temperatures and identifying potential hotspots or areas susceptible to overheating.
- To validate the simulation approach against analytically evaluated solutions, multiple test cases were conducted and reasonable agreement between the two approaches is achieved







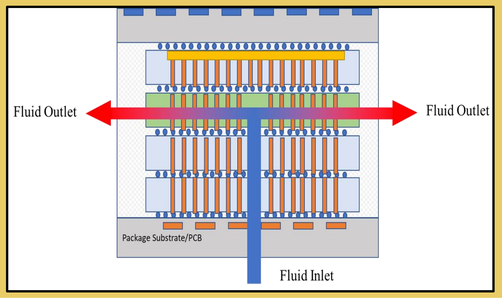


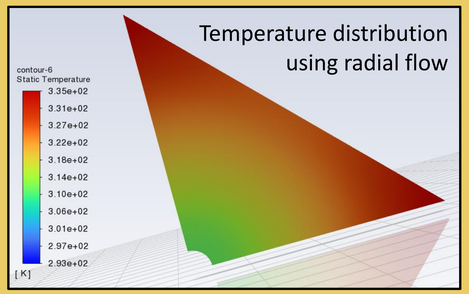
Results

- This study investigates microfluidic intralayer cooling techniques using analytical correlation and computational fluid dynamics (CFD) principles to propose a method capable of managing thermal performance across varying load conditions.
- The simulation results demonstrated that the proposed pin-fin arrangement would considerably reduce the silicon temperature by 11% relative to a hypothetical flow with no pin fins and while maintaining pressure drops lower than 350 kPa.
- The proposed configuration achieved a dissipation of 40 W/cm² with a volumetric flow rate of 200 mL/min, maintaining chip temperature at 315K.

Future Works

- Instead of linear flow, a radial flow of liquid coolant could be implemented which is expected to maintain lower chip temperature while maintaining a lower pressure drop
- From our initial simulation analysis, the radial arrangement showed 5% reduction in maximum temperature and 19% reduction in pressure drop.





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