Optimizing Compact Model of Nanosheet FET (NSFET) for Analog/Digital IC Design

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Driving question

A modern VLSI circuit contains more than a billion transistors in a single IC.
How can we accurately capture the behavior of nanoscale devices for advanced circuit and system design?

Background

- Compact Model is a bridge between IC design and semiconductor devices, which enables us to design and simulate circuit implementation to achieve desired functionality.
- Scaling to achieve faster, more energy-efficient devices as shown in Figure 1[1].
- The Nanosheet FET (NSFET) demonstrates superior performance, emerging as a leading option for 3 nm technology and beyond.
- Limited by reliability issues like transconductance degradation, parasitic from channel height and geometry of nanosheets, thermal effects.

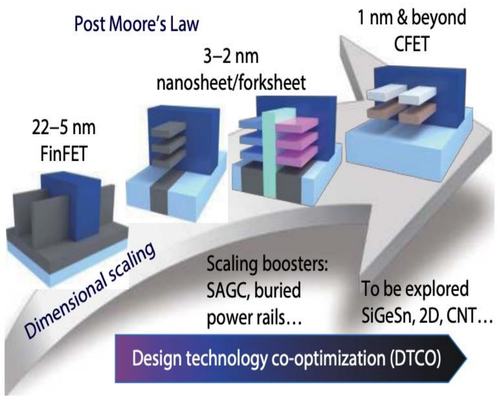


Fig1

Results

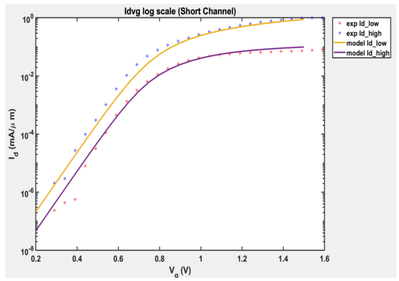


Fig3(a) [3]

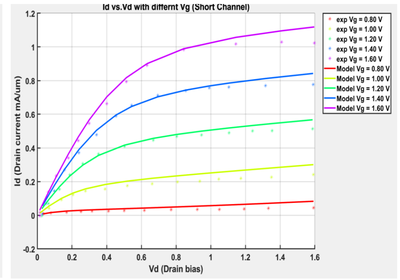


Fig3(b) [3]

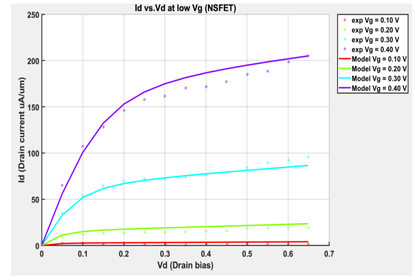
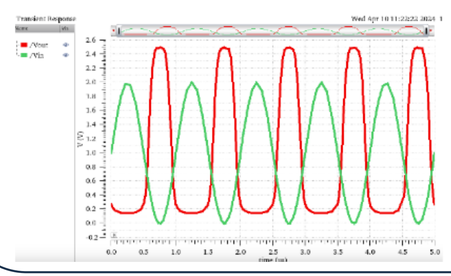
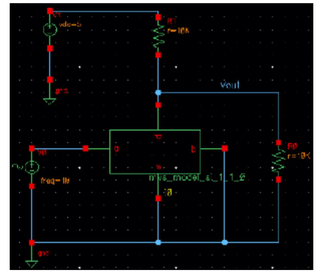


Fig4 [4]

Circuit level simulation





```
module mvs_si_1_1_0(d, g, s, b);
inout d, g, s, b;
electrical d, g, s, b;
electrical di, si;

// Original VS parameters
parameter real        version  = 1.10;
```

Goal

Developing a Compact model to accurately simulate the NSFET with desirable performance.

Process & Methods

- Extracting devices character with the **MIT Virtual Source (MVS) model**
  - Physical based model with Charge sheet approximation as fig.2[2].
  - Accurate short-channel phenomena such as DIBL, velocity saturation, etc.
  - Easily extracted with only 10 parameters needed.
  - Simplification through the virtual source concept for carrier injection modeling.

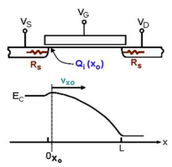


Fig2

Future works

1. Refine the MVS model for NSFET.
2. Continue research and study on Solid State Device Physics.
3. Integrate for system-level simulation..

FURI

Reference

[1]G. Han and Y. Hao, "Design technology co-optimization towards sub-3 nm technology nodes," Journal of Semiconductors, vol. 42, no. 2, pp. 020301–020301, Feb. 2021, doi: https://doi.org/10.1088/1674-4926/42/2/020301.
[2] Shaloo Rakheja; Dimitri Antoniadis (2015). MVS Nanotransistor Model (Silicon). (Version 1.1.1). nanoHUB. doi:10.4231/D3RR1PN6M
[3] L.-C. Wang et al., "Record Transconductance in Leff~30 nm Self-Aligned Replacement Gate ETSOI nFETs Using Low EOT Negative Capacitance HfO2-ZrO2 Superlattice Gate Stack," Jun. 2023, doi: https://doi.org/10.23919/vlsitechnologyandcir57934.2023.10185436.
[4] S. H. Lee et al., "High Performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template Assisted Selective Epitaxy," Dec. 2018, doi: https://doi.org/10.1109/iedm.2018.8614684.

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