Characterization of Synaptic Electronic Devices for Brain-Inspired Computing Systems

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Research Objective

Research question*: Are h-BN memristors promising candidates to implement brain-inspired computing devices and circuits?*

This semester's project investigates the h-BN memristor's ability **to perform the dot-product operation**, a function foundational to most machine learning algorithms.

Information gained will inform the viability of implementing complex neural networks in hardware.

2D Memristor Technology

Filament formation occurs by the penetration of titanium (Ti) ions into defects at h-BN grain boundaries by a positive voltage set signal. Filament dissolution is triggered by a negative reset signal.

2D materials allow scaling to the sub-nanometer level to enable device operation with low switching voltages and high programming speeds while maintaining efficiency.

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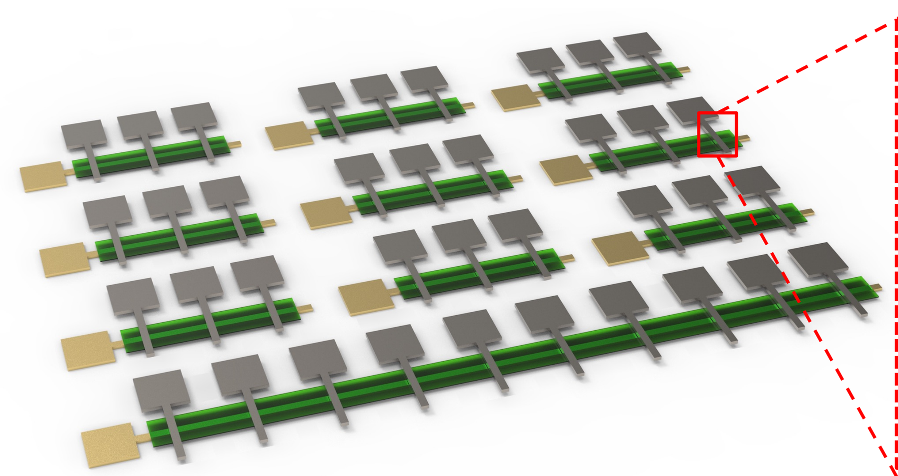

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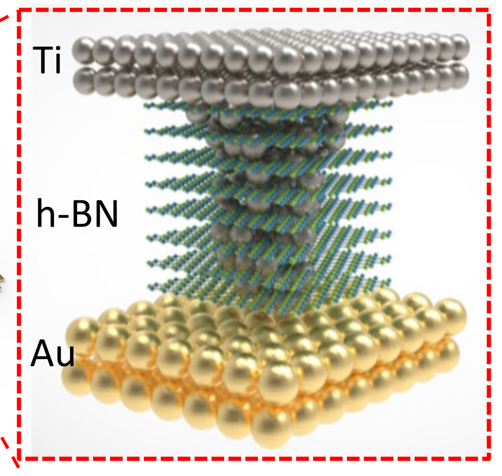

Figure 1: Schematic of the Au/h-BN/Ti memristor arrays; Figure 2: A representation of conductive nanofilaments on the Au/h-BN/Ti memristors.; Figure 3: Pulse programming of a single memristor device; Figure 4: Schematic of dot-product operation in an h-BN memristor array

Dot-Product Operation

In the dot-product operation, the product of the input voltage signals is multiplied by the conductances of the memristor arrays to accumulate an output current.

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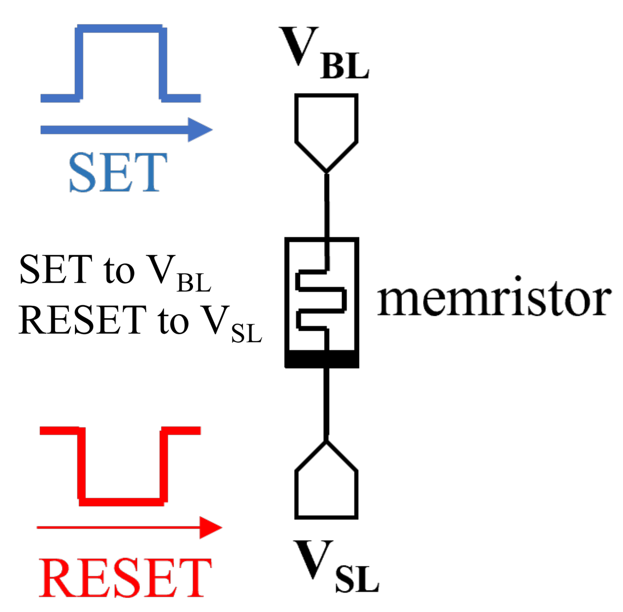

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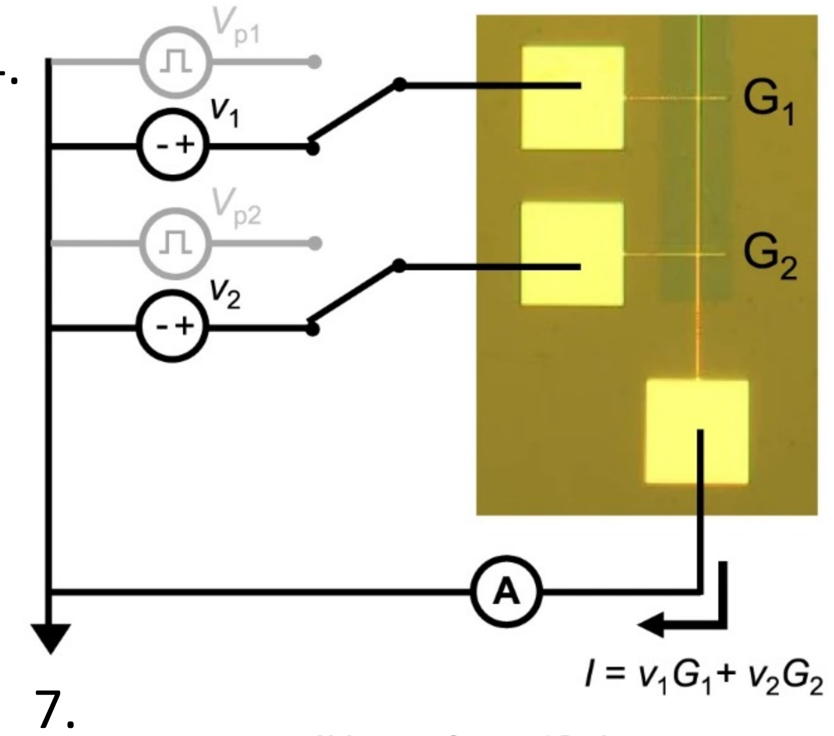

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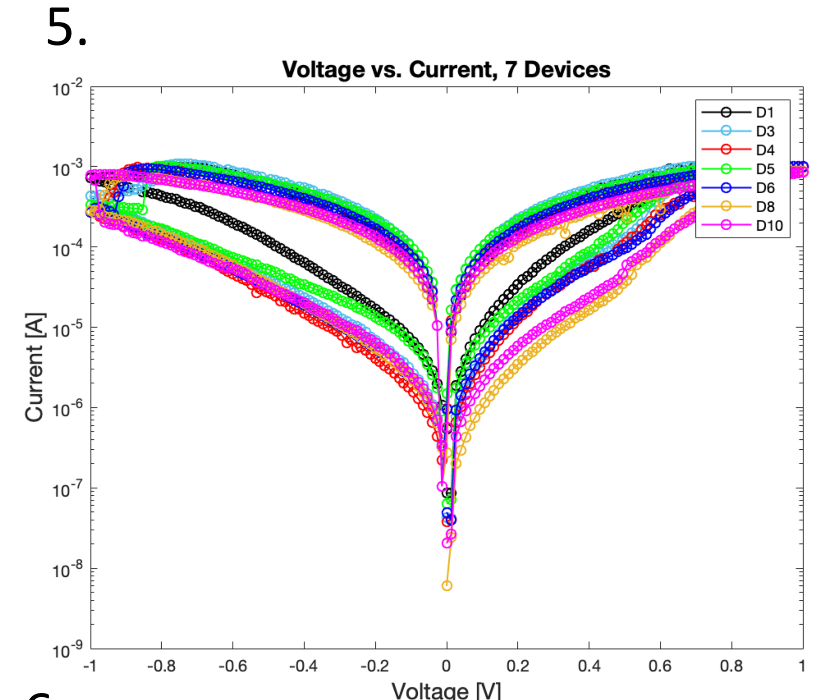

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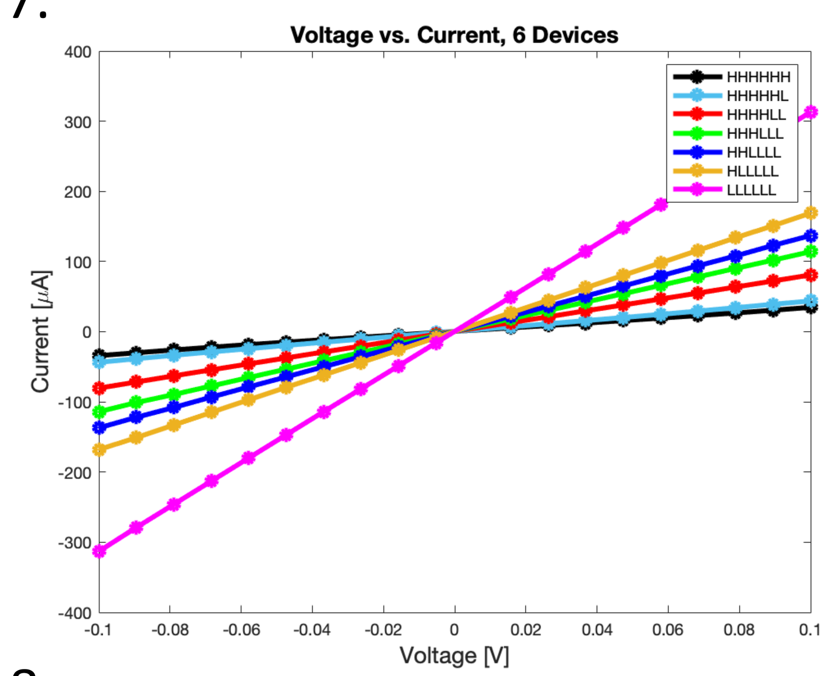

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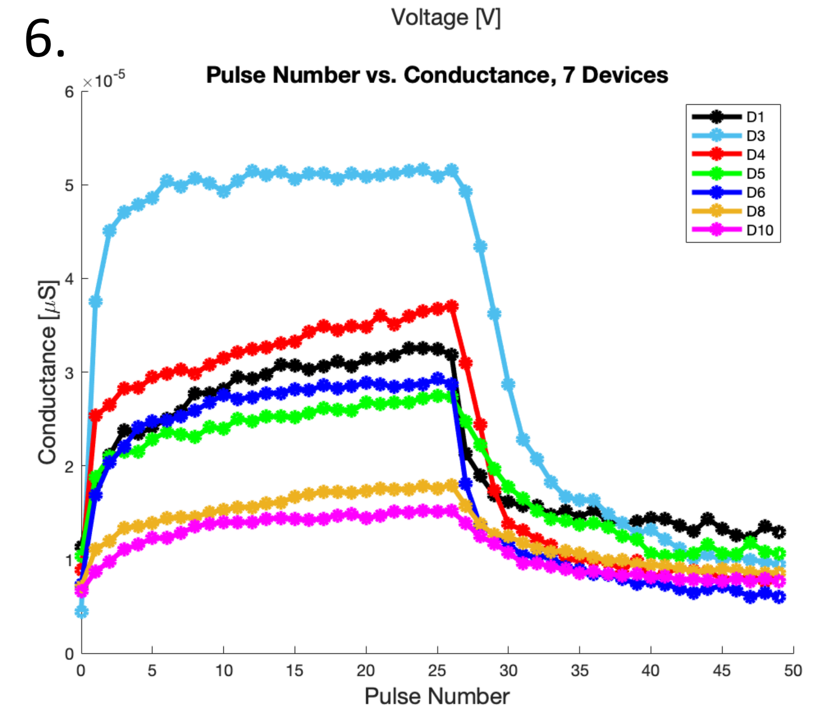

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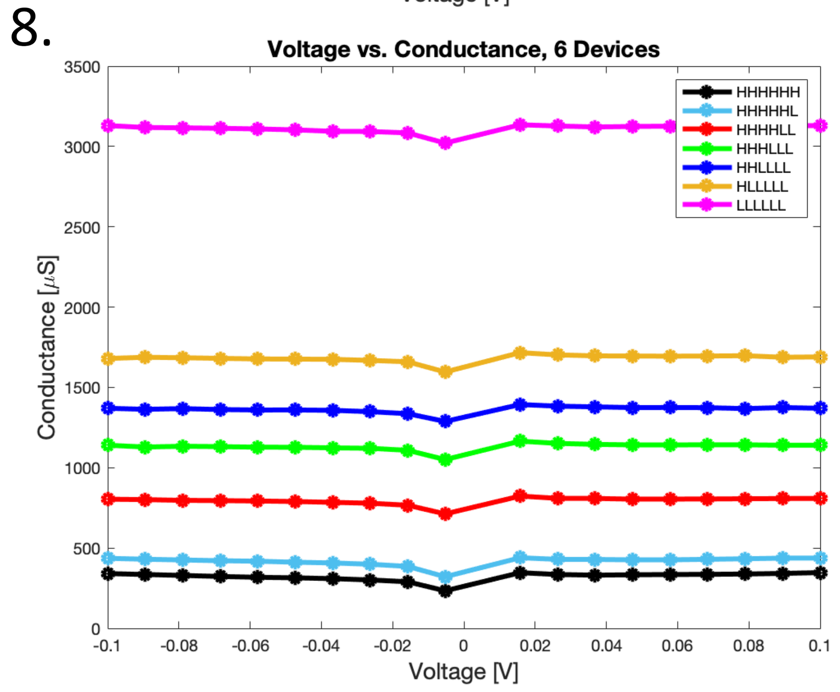
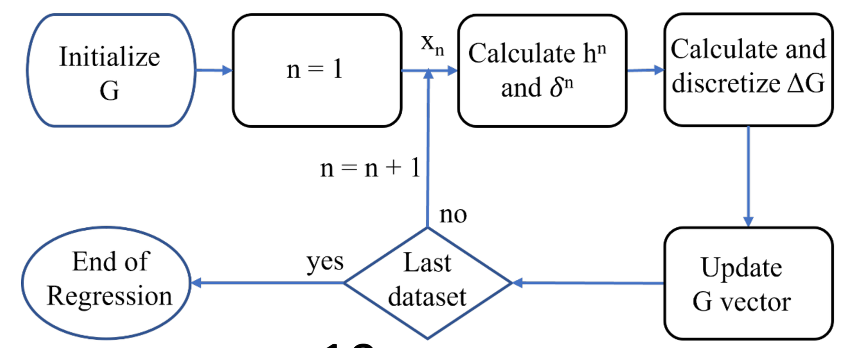


Figure 5: Dual sweep I-V characteristics curve; Figure 6: Pulsed programming curve; Figure 7: Dot-product implementation, voltage is swept after individual device transition from HRS to LRS; Figure 8: Plot of disparate conductance states after programming vs. voltage

Machine Learning Applications

Linear Regression



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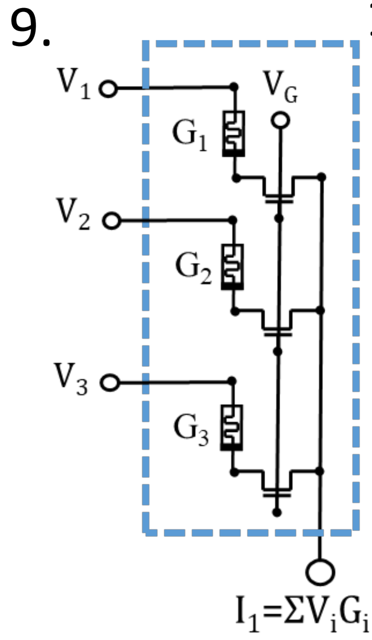

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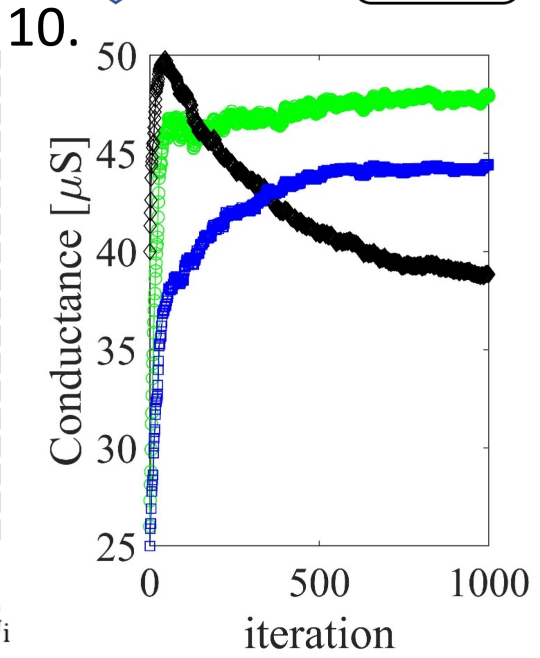

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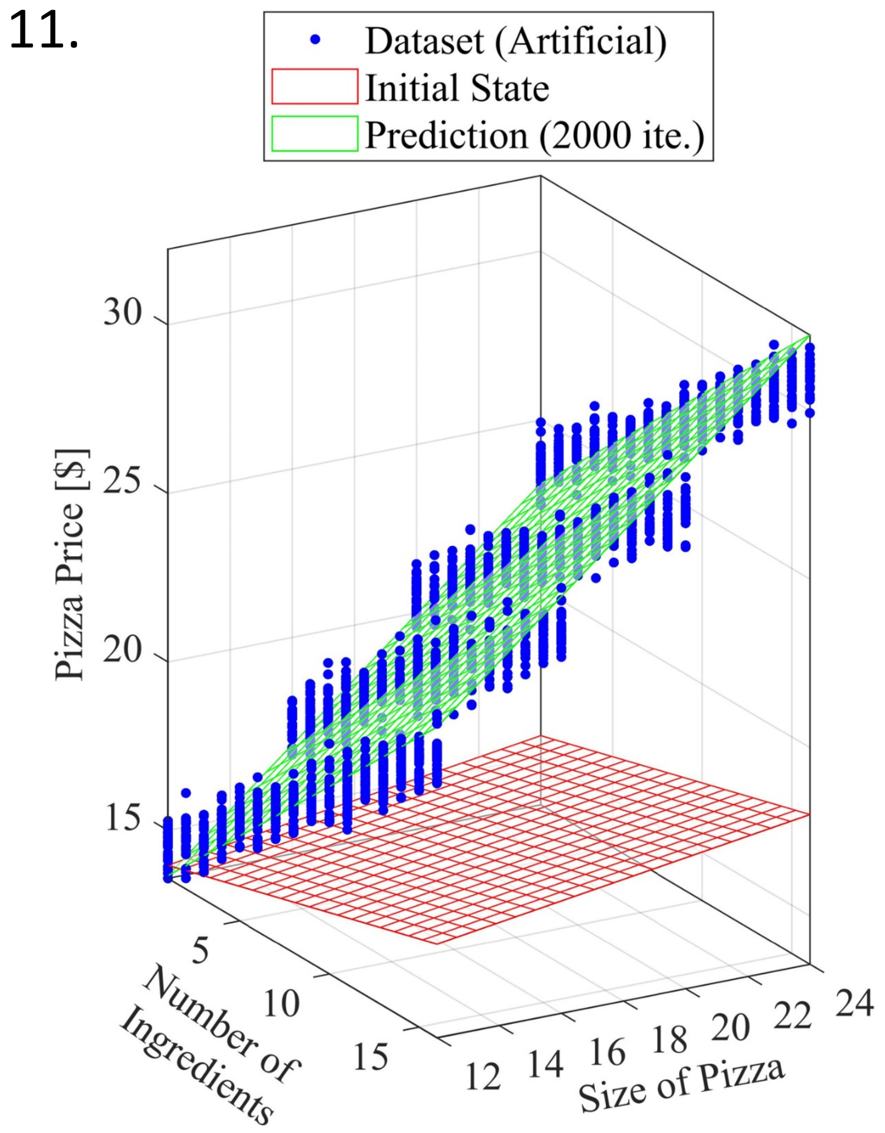
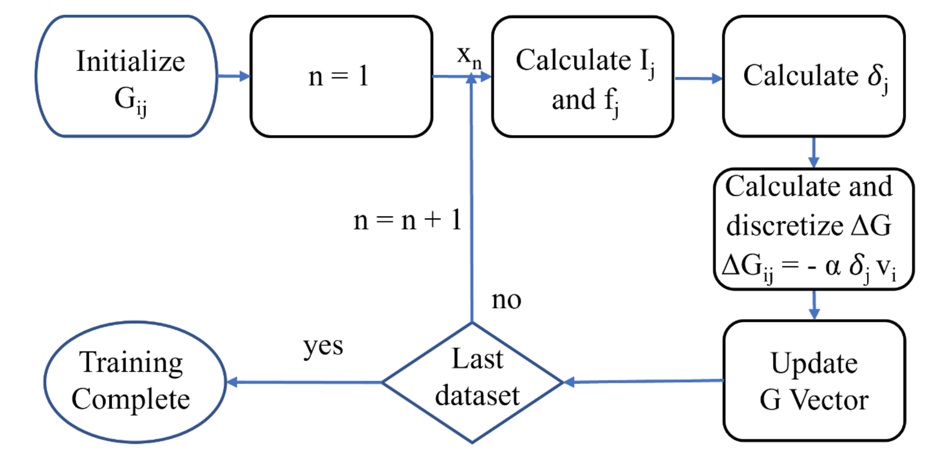


Figure 9: Schematic of the 3×1 crossbar; Figure 10: Conductance evolution for each memristor vs iteration; Figure 11: Results of linear regression algorithm on a memristor crossbar. Green mesh is the final prediction after 1000 iterations

Logistic Regression



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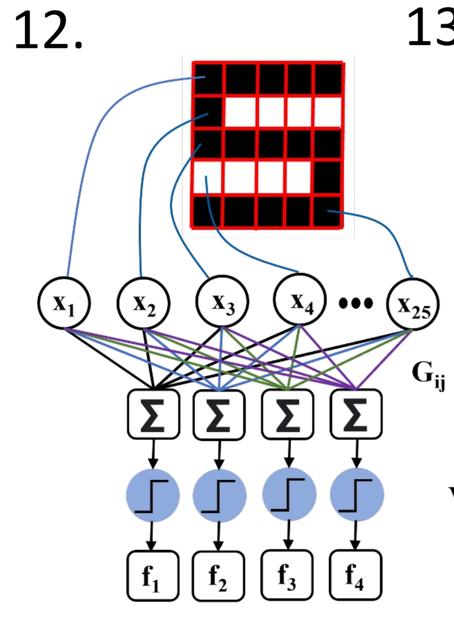

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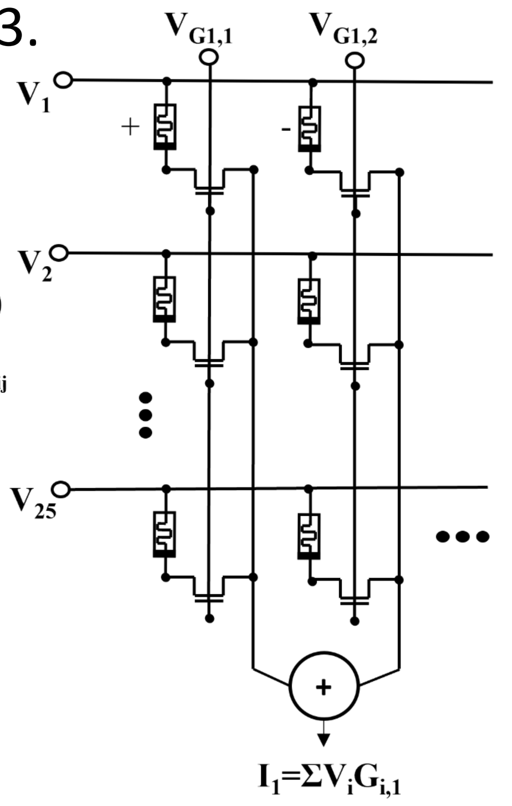

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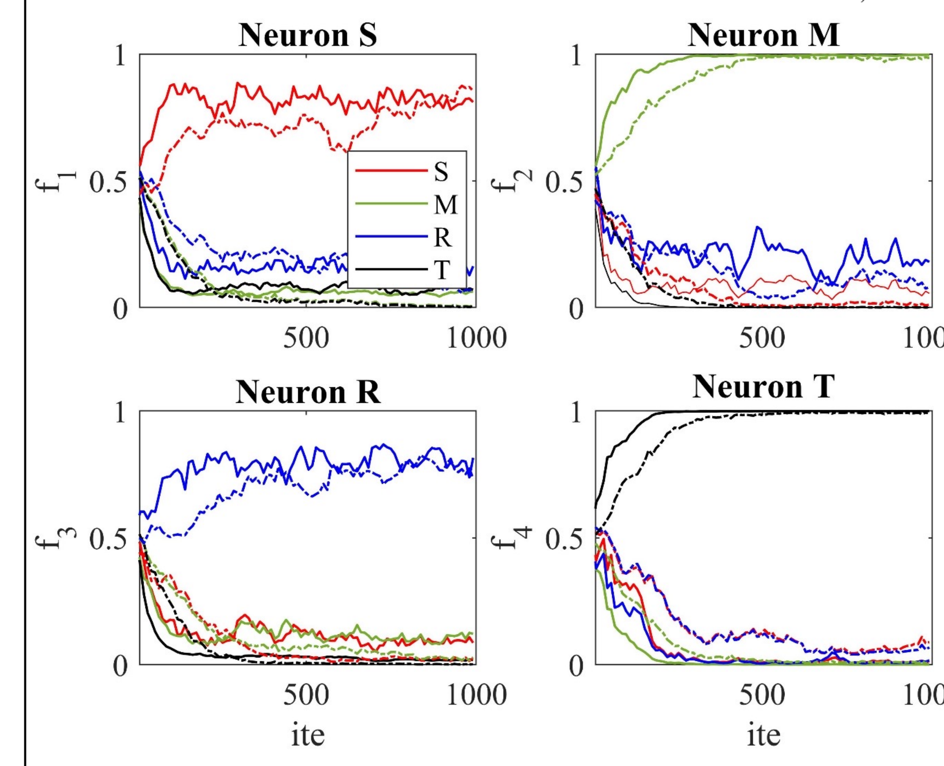

Figure 12: Graph representation of the neural network implementation for 5×5 input binary image (S, M, R, T) classification; Figure 13: Partial schematic of the 25×8 memristor crossbar for simulation of logistic regression; Figure 14: Evolution of convergence for each output neuron for logistic regression

References: [1] S. Afshari, M. Musisi-Nkambwe and I. Sanchez Esqueda, "Analyzing the Impact of Memristor Variability on Crossbar Implementation of Regression Algorithms With Smart Weight Update Pulsing Techniques," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 5, pp. 2025-2034, May 2022, doi: 10.1109/TCSI.2022.3144240.
[2] Xie, J., Afshari, S. & Sanchez Esqueda, I. Hexagonal boron nitride (h-BN) memristor arrays for analog-based machine learning hardware. *npj 2D Mater Appl* **6**, 50 (2022). https://doi.org/10.1038/s41699-022-00328-2

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